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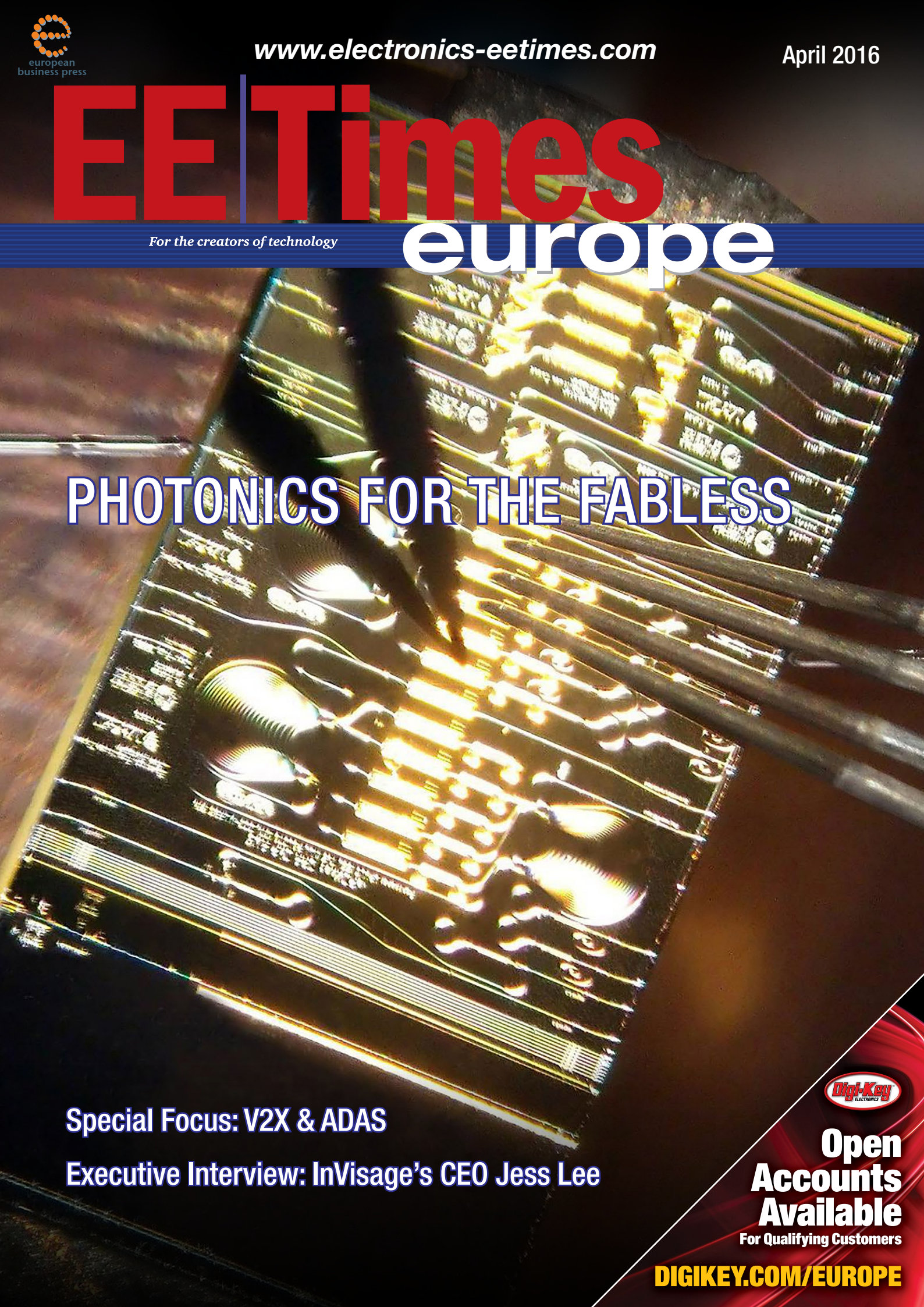

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Special Focus: V2X & ADAS

Executive Interview: InVisage's CEO Jess Lee

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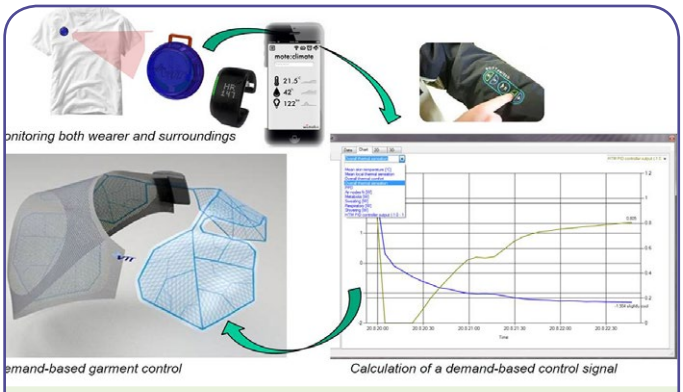
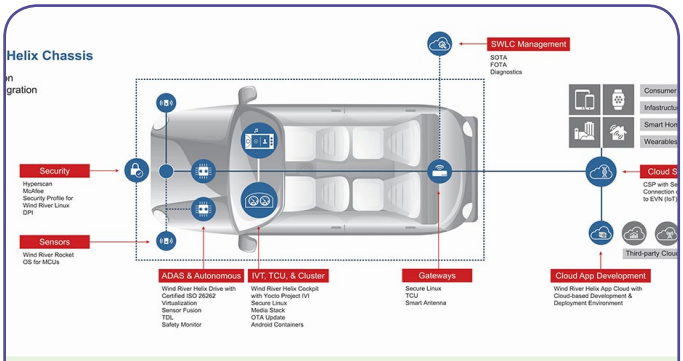
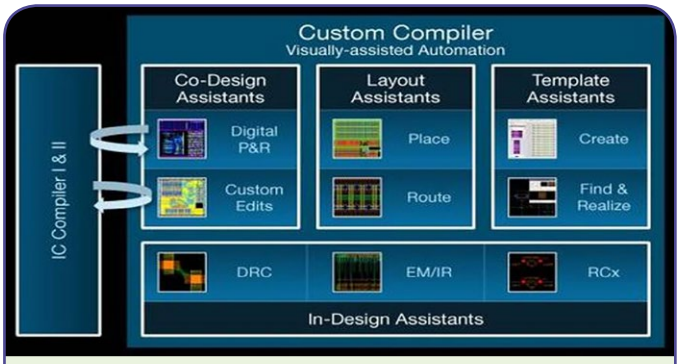
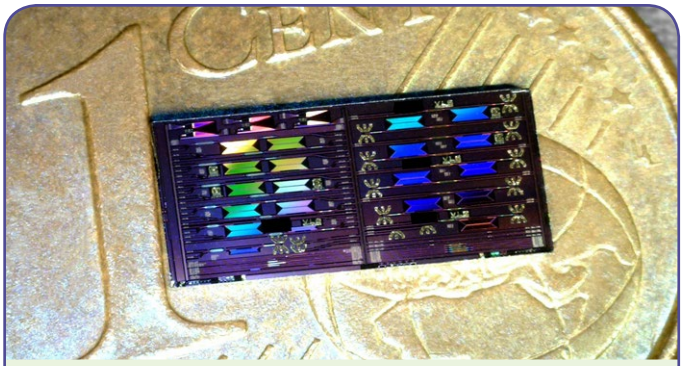








Smart clothing computes wearer's thermal needs

By Julien Happich

According to Pekka Tuomaala, Principal Scientist at the VTT Technical Research Centre of Finland, smart clothing of the future will automatically adjust their temperature to match the wearer's actual needs.

In November last year, the Finnish research center had unveiled one of the potential building blocks for such self-tuning thermally active clothes: microscopic channel networks hot embossed onto large areas of soft and elastic plastic film, through which cold or hot liquid could be pumped.

Integrated into smart clothing, the microfluidic channels are analogous to the cardiovascular system which irrigates different parts of the body (though it is the human metabolism which defines the blood's distribution at a given time).

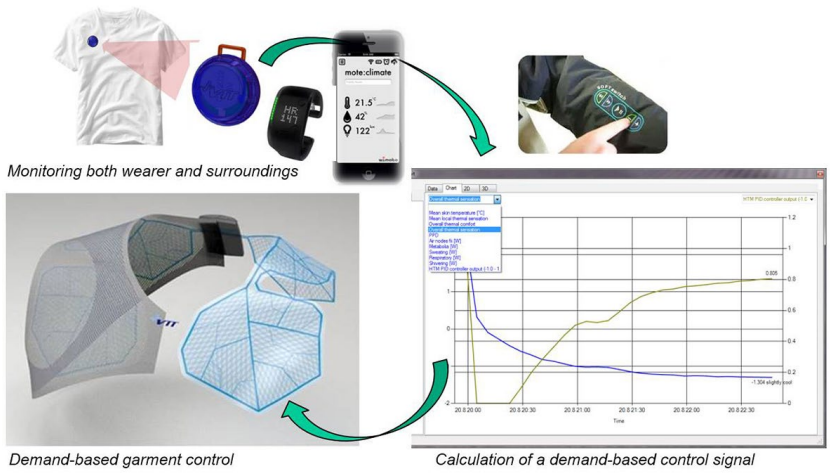
Prior research established that humans dissipates approximately 85% of their body's heat loss through the skin, so the smart irrigated fabric would act as not only a comfort layer but also double up as a thermoregulatory skin.

But before such "personalised air conditioning" smart fabrics can maintain the wearer's thermal comfort, they need to be able to regulate their temperature appropriately, so as to automatically adjust to external conditions.

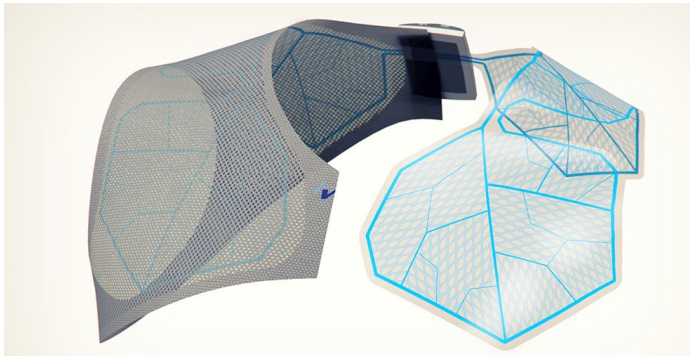
This calls for accurate human thermal model calculations, and the research lab has just developed the tools for that, enabling to correlate surrounding temperature and on-body temperature measurement with a person's thermal sensations.

As described in Riikka Holopainen's PhD dissertation, "A human thermal model for improved thermal comfort", the newly developed model takes into account the effect of human thermoregulation and individual human parameters on thermal sensation and comfort, to calculate more realistically the interaction and non-uniform transient heat transfer between the skin surface and the surrounding air and building structures.

Arguably, smart fabrics driven by such a model would require multiple temperature inputs, distributed around the wearer's body while also taking into account external temperature and the wearer's activity level (the human body continuously generates heat from about 75W during sleep to 1 000W during hard exercise). The algorithms may be further optimised for a given person's body mass index.



Concept of "personalised air conditioning" smart fabrics.

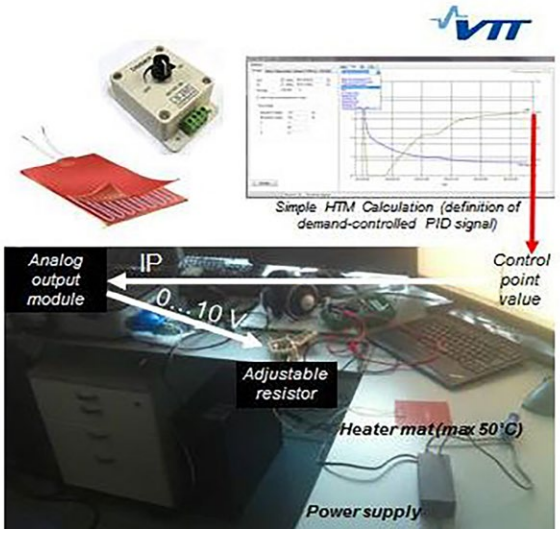


Microfluidic channels to be integrated into smart clothing, with a thermoregulator backpack.

The model's calculations aim to determine the needed warming or cooling power so that the thermal sensation of the person wearing the smart clothing remains optimal in varying conditions. Providing the smart fabrics are designed with both heating and cooling capabilities (maybe with a sort of miniature heat exchanger belt or backpack integrating Peltier elements and heated mats), such wearable technology could find applications across different consumer groups, including police officers, firemen, soldiers, outdoor workers, athletes, in-bound patients and small babies.

"Hospital patients have been asked about their most unpleasant experience, and the most common answer is feeling cold – pain comes only second", explains Principal Scientist Pekka Tuomaala from VTT. "For example, patients often feel cold after surgery. Body temperature can be individually adjusted, when a smart blanket identifies the person, measures the ambient temperature and adjusts the blanket's temperature to meet the patient's actual needs".

Still a small-scale lab experiment, Tuomaala has proven smart clothing control, showing in real-time the impacts of changes in ambient air temperature on the heating power of a small electrically heated mat. The lab has yet to establish the sort of control signals that would operate such smart fabrics, but it is looking for companies to further develop the technology.



Small-scale lab experiment showing in real-time the impacts of changes in ambient air temperature on the heating power of a small electrically heated mat.

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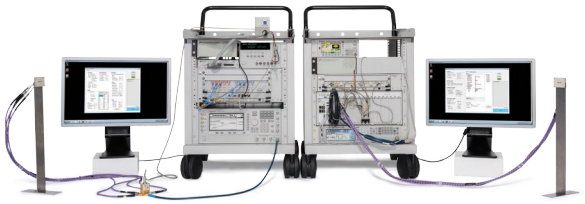

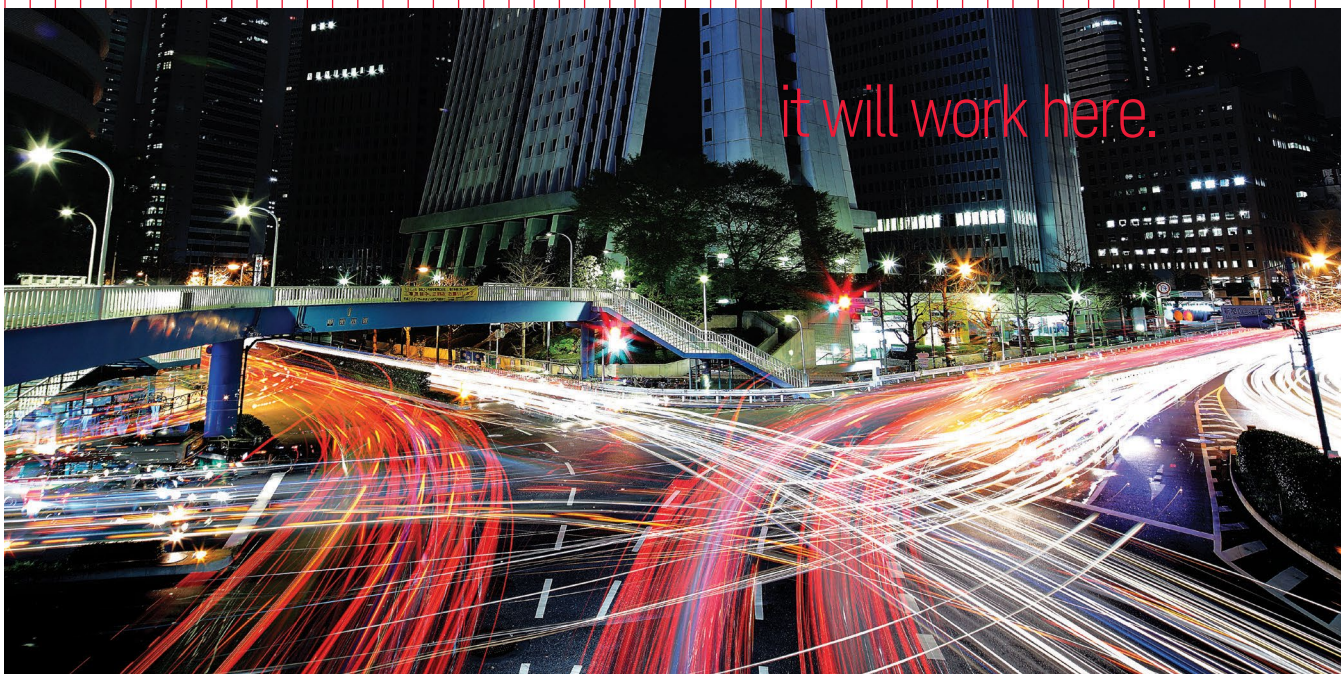

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Graphene-wrapped nanocrystals pushes fuel cell boundaries

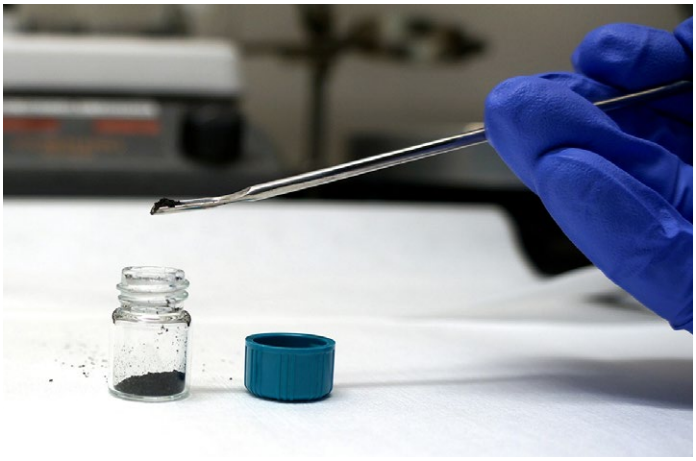
By Paul Buckley

Researchers at the U.S. Department of Energy's Lawrence Berkeley National Laboratory (Berkeley Lab) have developed a new materials recipe for a battery-like hydrogen fuel cell to push the device's performance forward in key areas.

The fuel cell design surrounds hydrogen-absorbing magnesium nanocrystals with atomically thin graphene sheets. The graphene shields the nanocrystals from oxygen and moisture and contaminants, while tiny, natural holes allow the smaller hydrogen molecules to pass through. The filtering process overcomes common problems degrading the performance of metal hydrides for hydrogen storage.

The graphene-encapsulated magnesium crystals act as 'sponges' for hydrogen, offering a compact and safe way to take in and store hydrogen. The nanocrystals also permit faster fueling, and reduce the overall 'tank' size.

"Among metal hydride-based materials for hydrogen storage for fuel-cell vehicle applications, our materials have good performance in terms of capacity, reversibility, kinetics and stability," said Eun Seon Cho, a postdoctoral researcher at Berkeley Lab and lead author of a study related to the new fuel cell formula, published recently in Nature Communications.



In a hydrogen fuel cell-powered vehicle using these materials, known as a 'metal hydride' (hydrogen bound with a metal) fuel cell, hydrogen gas pumped into a vehicle would be chemically absorbed by the magnesium nanocrystaline powder and rendered safe at low pressures.

"This work suggests the possibility of practical hydrogen storage and use in the future. I believe that these materials represent a generally applicable approach to stabilizing reactive materials while still harnessing their unique activity - concepts that could have wide-ranging applications for batteries, catalysis, and energetic materials," said Jeff Urban, a Berkeley Lab staff scientist and co-author.

The research, conducted at Berkeley Lab's Molecular Foundry and Advanced Light Source, is part of a National Lab Consortium, dubbed HyMARC (Hydrogen Materials - Advanced Research Consortium) that seeks safer and more cost-effective hydrogen storage, and Urban is Berkeley Lab's lead scientist for that effort.

The U.S. market share for all electric-drive vehicles in 2015, including full-electric, hybrids and plug-in hybrid vehicles, was 2.87 percent, which amounts to about 500,000 electric-drive vehicles out of total vehicle sales of about 17.4 million, according to statistics reported by the Electric Drive Transportation Association, a trade association promoting electric-drive vehicles. Hydrogen-fuel-cell vehicles have not yet made major in-roads in vehicle sales, though several major auto manufacturers including Toyota, Honda, and General Motors, have invested in developing hydrogen fuel-cell vehicles. Indeed, Toyota released a small-production model called the Mirai, which uses compressed-hydrogen tanks, last year in the USA.

A potential advantage for hydrogen-fuel-cell vehicles, in addition to their reduced environmental impact over standard-fuel vehicles, is the high specific energy of hydrogen, which means that hydrogen fuel cells can potentially take up less weight than other battery systems and fuel sources while yielding more electrical energy.

A measure of the energy storage capacity per weight of hydrogen fuel cells, known as the 'gravimetric energy density', is roughly three times that of gasoline. Urban noted that this important property, if effectively used, could extend the total vehicle range of hydrogen-based transportation, and extend the time between refueling for many other applications, too.

More R&D is needed to realize higher-capacity hydrogen storage for long-range vehicle applications that exceed the performance of existing electric-vehicle batteries, Cho said, and other applications may be better suited for hydrogen fuel cells in the short term, such as stationary power sources, forklifts and airport vehicles, portable power sources like laptop battery chargers, portable lighting, water and sewage pumps and emergency services equipment.

Cho said that a roadblock to metal hydride storage has been a relatively slow rate in taking in (absorption) and giving out (desorption) hydrogen during the cycling of the units. In fuel cells, separate chemical reactions involving hydrogen and oxygen produce a flow of electrons that are channelled as electric current, creating water as a by-product.

The tiny size of the graphene-encapsulated nanocrystals created at Berkeley Lab, which measure only about 3-4 nanometers, is a key in the new fuel cell materials' fast capture and release of hydrogen, Cho said, as they have more surface area available for reactions than the same material would at larger sizes. Another key is protecting the magnesium from exposure to air, which would render it unusable for the fuel cell, added Cho.

Working at The Molecular Foundry, researchers found a simple, scalable and cost-effective 'one pan' technique to mix up the graphene sheets and magnesium oxide nanocrystals in the same batch. They later studied the coated nanocrystals' structure using X-rays at Berkeley Lab's Advanced Light Source. The X-ray studies showed how hydrogen gas pumped into the fuel cell mixture reacted with the magnesium nanocrystals to form a more stable molecule called magnesium hydride while locking out oxygen from reaching the magnesium.

"It is stable in air, which is important," said Cho.

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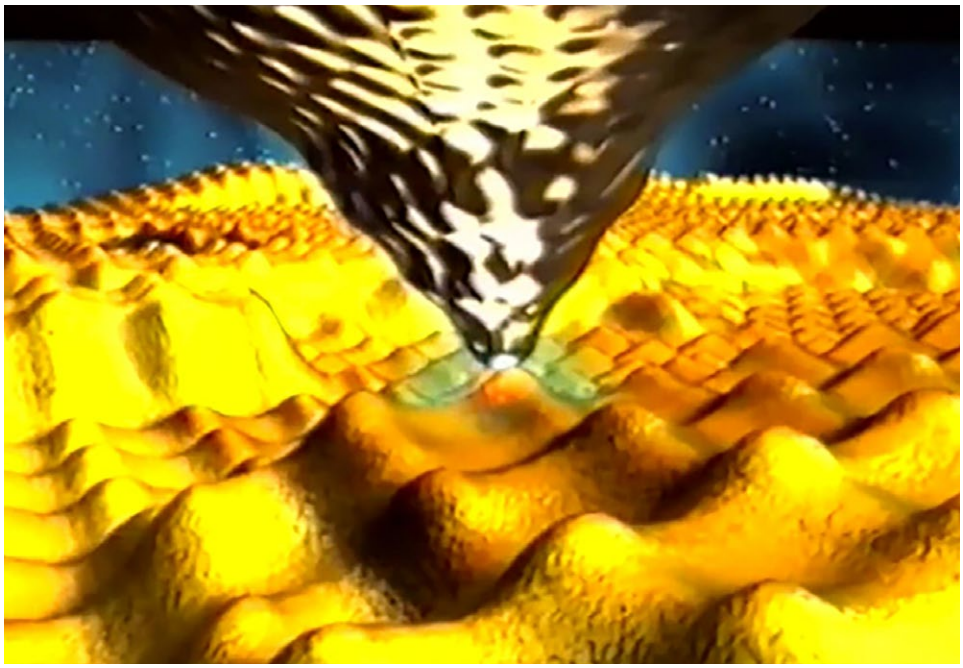
IBM pioneers nanoscale thermometry

By Paul Buckley

Scientists from IBM and ETH Zurich have invented a technique to measure the temperature of nanoscale objects - a key challenge in nanoscience - which could pave the toward being able to precisely characterize the temperature of new transistor designs to meet the demand of future cognitive computers. The patent-pending invention has been described in the peer-review journal Nature Communications in a paper titled 'Temperature mapping of operating nanoscale devices by scanning probe thermometry.' The nanoscale measurement technique comes from the IBM lab which was previously responsible for inventing the scanning tunnelling microscope and the atomic force microscope.

Accurately measuring the temperature of objects at the nanoscale has been challenging scientists for decades. Current techniques are not accurate and they typically generate artefacts, limiting their reliability.

In the 1980s, IBM scientists Gerd Binnig and the late Heinrich Rohrer wanted to directly explore a surface's electronic structure and imperfections. The instrument they needed to take such measurements didn't exist, yet. So they did what any good scientist would do: they invented one. It became known as the scanning tunnelling microscope (STM), opening the door to nanotechnology. More than 30 years later IBM scientists continue to follow in the footsteps of Binnig and Rohrer and with their latest invention.



"We started back in 2010 and simply never gave up.

Previous research was focused on a nanoscale thermometer, but we should have been inventing a thermometer for the nanoscale—an important distinction. This adjustment led us to develop a technique which combines local thermal sensing with the measuring capability of a microscope—we call it scanning probe thermometry," says Dr. Fabian Menges, an IBM postdoc and co-inventor of the technique.

The most common technique to measure temperature on the macroscale is to bring a thermometer into thermal contact with the sample. This is how a fever thermometer works. Once it's placed under our tongue it equilibrates to our body temperature so that we can determine our temperature at a healthy 37°C.

Unfortunately, it gets a little more challenging when using a thermometer to measure a nanoscopic object. For example, it would be impossible to use a typical thermometer to measure the temperature of an individual virus. The size of the virus is too small and the thermometer cannot equilibrate without disturbing the virus temperature.

To solve the challenge, IBM scientists developed a single scan non-equilibrium contact thermometry technique to measure the temperature of nanoscopic objects using a scanning probe. As the scanning probe thermometer and the object cannot thermally equilibrate at the nanoscale, two signals are measured simultaneously: a small heat flux, and its resistance to heat flow. Combining the two signal the temperature of nanoscopic objects can then be quantified for an accurate result.

"The technique is analogous to touching a hot plate and inferring its temperature from sensing the heat flux between our own body and the heat source. Essentially, the tip of the probe is our hand. Our perception to hot and cold can be very helpful to get an idea of an objects temperature, but it can also be misleading if the resistance to heat flow is unknown," explained IBM scientist Dr. Bernd Gotsmann and co-inventor.

Previously, scientists were not accurately including this resistance dependence; but only measuring the rate of the thermal energy transfer through the surface, known as heat flux. In the paper, the authors included the effects of local variations of thermal resistance to measure the temperature of an indium arsenide (InAs) nanowire, and a self-heated gold interconnect with a combination of a few milli Kelvin and few-nanometer spatial resolution.

"Not only is the scanning probe thermometer accurate, it meets the trifecta for tools: it's easy to operate, simple to build, and very versatile, in that it can be used to measure the temperature of nano- and micro-sized hot spots that can locally effect the physical properties of materials or govern chemical reactions in devices such as transistors, memory cells, thermoelectric energy converters or plasmonic structures. The applications are endless," says Menges.

The team began to see improvements in the development of the scanning probe thermometer 18 months ago when they moved their research into the new Noise Free Labs — six meters underground at the Binnig and Rohrer Nanotechnology Center on the campus of IBM Research-Zurich.

The environment, which shields the experiments from vibration, acoustic noise, electromagnetic signals and temperature fluctuations, helped the team achieve sub-milli Kelvin precision.

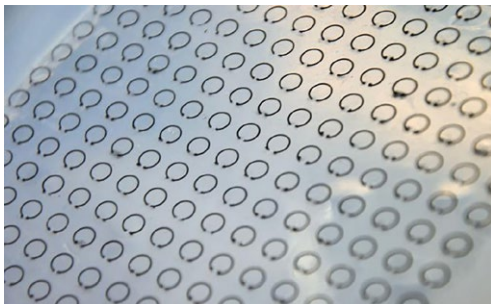
"While we had the benefit of this unique room, the technique can also produce reliable results in normal environment," says Menges.

Stretchable skin traps radar waves

By Jean-Pierre Joosting

A flexible, stretchable and tuneable "meta-skin" that uses rows of small, liquid-metal devices to cloak an object from the sharp eyes of radar has been developed by Iowa State University engineers. The metamaterial can be tuned to reduce the reflection of a wide range of radar frequencies by controlling the stretching and flexing of the polymer meta-skin.

"It is believed that the present meta-skin technology will find many applications in electromagnetic frequency tuning, shielding and scattering suppression," the engineers wrote in their paper, published in the journal Scientific Reports.



This flexible, stretchable and tuneable "meta-skin" can trap radar waves and cloak objects from detection. Image courtesy of Liang Dong, Iowa State University.

To prove the idea that electromagnetic waves — and perhaps even the shorter wavelengths of visible light — can be suppressed with flexible, tuneable liquid-metal technologies, the researchers implemented rows of split ring resonators embedded inside layers of silicone sheets. The electric resonators are filled with galinstan, a metal alloy that's liquid at room temperature and less toxic than other liquid metals such as mercury.

Those resonators are small rings with an outer radius of 2.5 millimeters and a thickness of half a millimeter. They have a 1 millimeter gap, essentially creating a small, curved segment of liquid wire.

The rings create electric inductors and the gaps create electric capacitors. Together they create a resonator that can trap and suppress radar waves at a certain frequency. Stretching the meta-skin changes the size of the liquid metal rings inside and changes the frequency the devices suppress.

Tests showed radar suppression was about 75 percent in the frequency range of 8 to 10 gigahertz, according to the paper. When objects are wrapped in the meta-skin, the radar waves are suppressed in all incident directions and observation angles.

According to the paper this meta-skin technology is different from traditional stealth technologies that often only reduce the backscattering (the power reflected back to a probing radar).

"The long-term goal is to shrink the size of these devices," said Dong, one of the lead authors. "Then hopefully we can do this with higher-frequency electromagnetic waves such as visible or infrared light. While that would require advanced nanomanufacturing technologies and appropriate structural modifications, we think this study proves the concept of frequency tuning and broadening, and multidirectional wave suppression with skin-type metamaterials."

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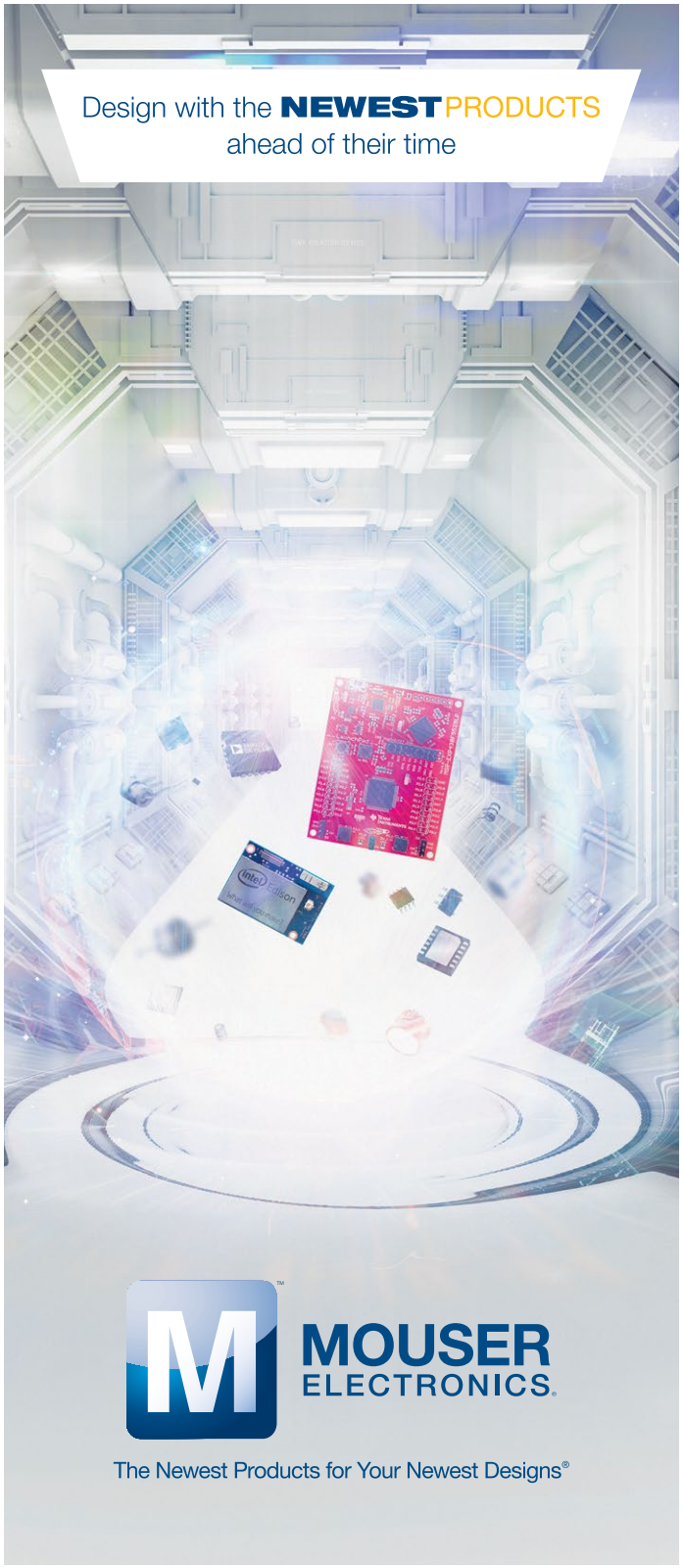

Startup InVisage's CEO: why image sensor revolution is upon us

By Peter Clarke

EE Times Europe interviewed InVisage CEO Jess Lee and asked him to explain why he feels his startup company is on the verge of great things in the image sensor market, and potentially elsewhere.

InVisage Technologies Inc. (Menlo Park, Calif.) is an image sensor startup that is nearly ten years old and that has taken in more than $100 million in venture capital. The company has been developing image sensors based on a quantum-dot material called QuantumFilm that replaces conventional silicon photodiodes but that is integrated on supporting CMOS technology.

It now has two products out in the market and is starting to gain traction, according to Lee.

EE Times Europe: What is QuantumFilm made of and how does it differ from other quantum dot materials?

Jess Lee: "We have not said too much about the material structure of QuantumFilm. There are concerns over cadmium in quantum dots so the first thing to say is there is no cadmium. What we have said is that it is a metal-chalcogenide material, similar to a II-VI material surrounded by ligands in a matrix."

Lee added that it is the combination of the quantum dots and the carrier material that allows charge transfer. "It's because of the packing regime we are in." The dots are of a diameter of between about 3-micron and 5-micron and it is these dimensions that affect the electron band structure and govern the sensitivity to light.

In addition, InVisage has developed an automated process to control the diameter of quantum dots produced as part of film production, Lee said.

EETE: Quantum dots are known for having multiple applications besides sensing, such as displays and energy storage. Is InVisage only interested in image sensor applications?

JL: "Image sensors are our focus for the short- and medium-term future. It is where our expertise is. But semiconductor development is getting harder and More-than-Moore opportunities are increasing, so there is the possibility it [QuantumFilm] can be applied elsewhere in the future.

EETE: InVisage has been shown that QuantumFilm has certain advantages over silicon photodiodes in a number of parameters, such as sensistivity, viewing angle, but how does it compare in terms of speed?

JL: Lee answered by saying that for machine vision applications it may well be speed of response, rather than resolution, and other features such as global shutter that determine design wins. Lee pointed out that QuantumFilm is not limited in terms of its speed of response.

"We are limited by the state of silicon I/O and analog-to-digital converters. As that rises we can go at hundreds, even thousands of frames per second. There is no difference between us and comparable CMOS image sensors.

However, Lee said that QuantumFilm has an additional advantage: that it is able to capture scenes very quickly, in periods of the order of a millisecond, and apply a "global shutter" electronically. This is not done easily in CMOS image sensors, which conventionally use a scheme of continuously rolling exposure and line-by-line read out. Although this is adequate for still images it can produce visual artifacts in images of fast moving objects.

Jess Lee, CEO InVisage Technologies Inc.

EETE: CMOS image sensor manufacturing is mature and optimized for volume production and low unit costs. Surely InVisage cannot compete on price, as it is yet to build up volume sales and so must compete on performance? So can InVisage go after the smartphone mass market immediately?

JL: "The QuantumFilm does cost something but we have shown that this is viable in high volume. And we get the great optimization that TSMC can bring. So in the material we have something exclusive that we can make on a very high volume platform."

Lee points out that QuantumFilm sensors are not the same as CMOS image sensors and that the smartphone market is itself dynamic and is looking for superior performance. "The space we are in is performance and value add, but the primary motivation is performance."

And as with most engineering, the devil is in the detail. Most CMOS image sensors used in smartphones use thinned wafers and back-side illumination (BSI) "We don't require a BSI process which is also a fundamental cost advantage," said Lee.

So as to whether InVisage go after the smartphone market from its market debut, Lee said: "Yes. We have and we are. But we are also going after the machine vision market."

EETE: The CMOS image sensor market is reckoned to have been worth about $10 billion in 2015 and on a compound annual growth rate of about 11 percent. What penetration pattern do you envisage for QuantumFilm over time?

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JL: "We are aggressive in how we attack the market and integrate in product form but we also realise we can't bite off the whole market by ourselves. We're still a venture-backed startup. We can't build 20 fabs to produced QuantumFilm sensors. But we are looking to raise money with partners as investors," said Lee.

Lee added: "We see QuantumFilm as a platform used by us as the first and second customer. To have third and fourth customers is better for us. We are prepared to work with partners to enable them, with QuantumFilm. We wouldn't license the technology out but there are a number of other ways to enable partners." Lee said it was too early to name any potential customers for QuantumFilm or potential partners and investors.

EETE: Is there more engineering that can be done with QuantumFilm besides replacing silicon photodiodes in an array?

JL: "Absolutely there is. Near-infrared is something we are doing. Deploying multiple sensors with computational processing is possible although it is orthogonal to us. But we have a lot of latitude because we are on CMOS." Lee added that, in addition, InVisage customers are telling him that the global shutter capability makes it easier to do multi-sensor imaging because it aids synchronization of images.

"The product roadmap has two arcs; Pushing QuantumFilm and its performance and spectral range. The second arc is to build in the silicon. At the moment that is the readout circuit but there is no reason to stay there. We can also approach from the opposite direction. We can put QuantumFilm on other circuits. And we could also do optical sensors for ambient light, infrared for simple sensing," said Lee.

EETE: InVisage has raised more than $100 million in venture capital. How can you pay those investors back?

JL: "It's true the conventional semiconductor sector is a jungle with companies fighting at the leading edge.

This is one of the reasons venture capital has turned away from that sector. But we are on a mature silicon platform – 110nm. It's a very different capital investment process there. We have our own fab in Taiwan but it is only focused on a couple of processes – a spin-on process to add the film and the definition of the pixels."

But Lee is confident that it is possible for startups to be successful and reward their investors. Lee cites Ambarella Inc. (Santa Clara, Calif.) a developer of video compression and image processing products, and InvenSense Inc. (San Jose, Calif.), a provider of MEMS-based inertial sensor components and sub-systems. These companies were founded in 2004 and 2003 respectively and are both now publicly owned.

"Ultimately it [paying investors back] is only achieved by making product and making it competitive, but to this we have added that we don't just want to be a product company. We will provide our technology platform as well," said Lee.

Transparent wood could lower cost of solar cells

By Paul Buckley

Researchers at Stockholm's KTH Royal Institute of Technology have developed a transparent wood material that is suitable for mass production applications thereby offering the potential to lower solar cell manufacturing costs.

Lars Berglund, a professor at Wallenberg Wood Science Center at KTH, said that although optically transparent wood has been developed for microscopic samples in the study of wood anatomy, the KTH project introduces a way to use the material on a large scale. The finding was published in the American Chemical Society journal, Biomacromolecules.

"Transparent wood is a good material for solar cells, since it's a low-cost, readily available and renewable resource," said Berglund. "This becomes particularly important in covering large surfaces with solar cells." Transparent wood panels can also be used for windows, and semi-transparent facades, when the idea is to let light in but maintain privacy.

The optically transparent wood is a type of wood veneer in which the lignin, a component of the cell walls, is removed chemically. "When the lignin is removed, the wood becomes beautifully white.

But because wood isn't not naturally transparent, we achieve that effect with some nanoscale tailoring," explained Berglund.

The white porous veneer substrate is impregnated with a transparent polymer and the optical properties of the two are then matched. "No one has previously considered the possibility of creating larger transparent structures for use as solar cells and in buildings," said Berglund. "Wood is by far the most used bio-based material in buildings. It is attractive that the material comes from renewable sources. It also offers excellent mechanical properties, including strength, toughness, low density and low thermal conductivity."

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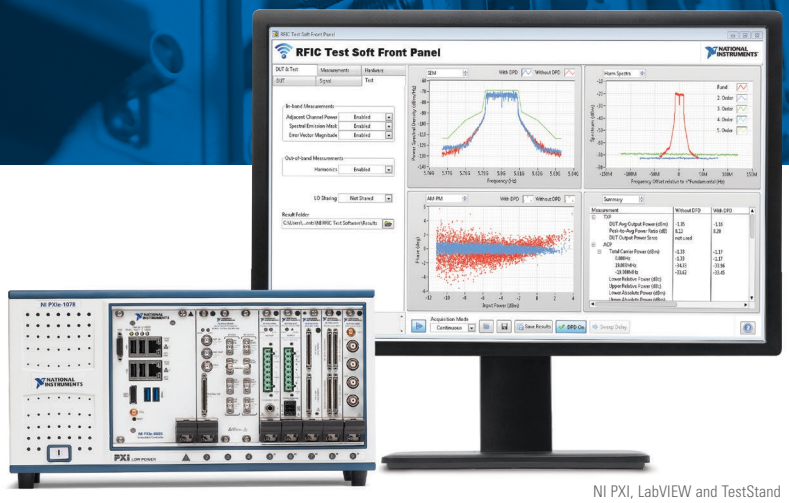

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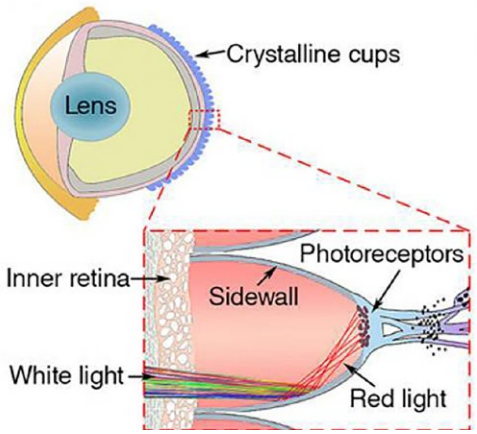
Bio-inspired lens gives image sensors night vision capability

By Julien Happich

While low-light imaging typically involves a race for better image sensor pixel design or the search for new photo-conversion materials with better light sensitivity, engineers from the University of Wisconsin–Madison have found their inspiration in nature to design a unique optical lens that dramatically increases the overall light input to a sensor.

The inspiration came from a combination of the Lobster's superposition compound eyes and the retinal structure of the small elephantnose fish, the later featuring thousands of crystalline cups covering its inner retina.



Schematic illustrations and images of a natural eye of elephantnose fish and an artificial eye.

In a paper titled "Artificial eye for scotopic vision with bioinspired all-optical photosensitivity enhancer", the researchers unveil an optical lens made out of thousands of micro-photocollectors (μ-PCs), each consisting of a tiny glass pillar with parabolic reflective sidewalls that focus the faint incoming light through it's the μ-PC's output port. The micro-photocollectors are arranged on a dome-shaped structure, so as to mimic the lobster's superposition compound eye where multiple light input ports concentrate the incoming light onto individual sensor pixels.

Using this unique lens, the researchers reported a four-fold improvement in light sensitivity when imaging objects in what could be described as pitch-black darkness. To manufacture the minuscule parabolic side-walled μ-PCs only about 120μm tall, the engineers relied on a hybrid laser ablation process.

"First, we use laser ablation to form the parabolic micro-cup structures in glass. Then we smoothen the sidewall surface by reflowing Su-8 photoresist, followed by coating aluminium as the reflective (mirror) layer", explained Hongrui Jiang, professor of electrical and computer and biomedical engineering at UW–Madison and the corresponding author on the study.

These micro-cups are then transferred to a 300μm thick PDMS hemispheric membrane to create the so-called bioinspired photosensitivity enhancer (BPE), in effect a fish-lens which can be used to boost just any imaging system, regardless of the imaging sensors in use.

As demonstrated through ray-tracing models, each μ-PCs collects the incoming light and concentrates the rays through reflection on the four parabolic sidewalls, to the narrower output port (going from a 77μm input port to a 20μm output port).

Because the closely packed μ-PCs are omni-directionally arranged on the hemispheric lens, the whole structure functions as a superposition compound eye with multiple incoming light ports for each pixel on the imager.

To validate the concept, the researchers designed a full fish-eye featuring a ball lens at the centre of a 8mm diameter iris, to generate a hemispherical image plane on a 48×48 array of μ-PCs laid out on the inside of a 25mm diameter dome (the PDMS hemispheric membrane).

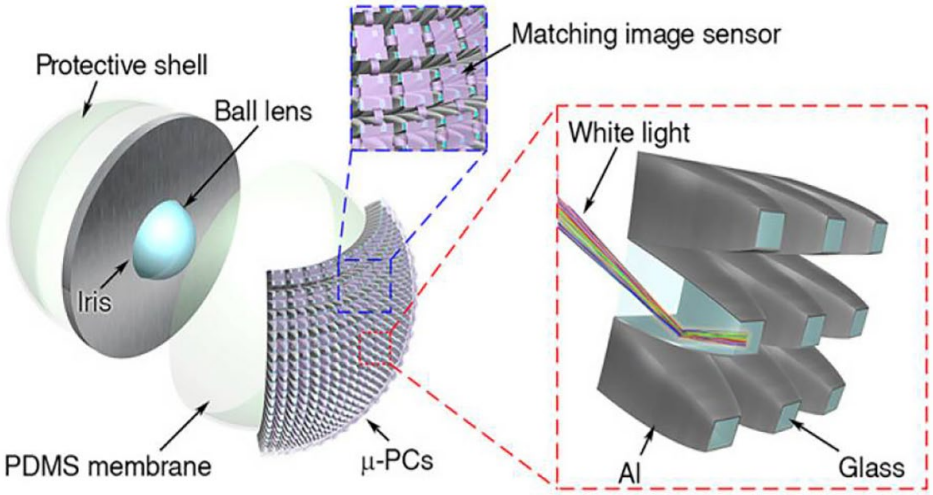
They used multiple step image capture and super-resolution image reconstruction algorithms to compensate for the superposition compound eye's intrinsic blur to produce crisp, clear pictures.

Would Jiang and his team expect further light concentration by simply scaling down these micro-mirror patterns?

"We studied the geometry effect of the cup structures. The dimension is not totally optimized, but it did consider these geometry effects. Too small a structure would have diffraction, though, so it might not work better" answered Jiang who hopes to further develop the technology for its commercialization, most probably through IP licensing.

As for mass manufacture, "The moulding process might work well. That is, using laser ablation to create a master and then use that to mould the micro-cup array. Nano imprint might not work, though, as we are talking about 10's of micron in width and about 100 micron in depth", clarified the researcher.

On top of this all-optical light concentration, would it be conceivable to include some form of light amplification through



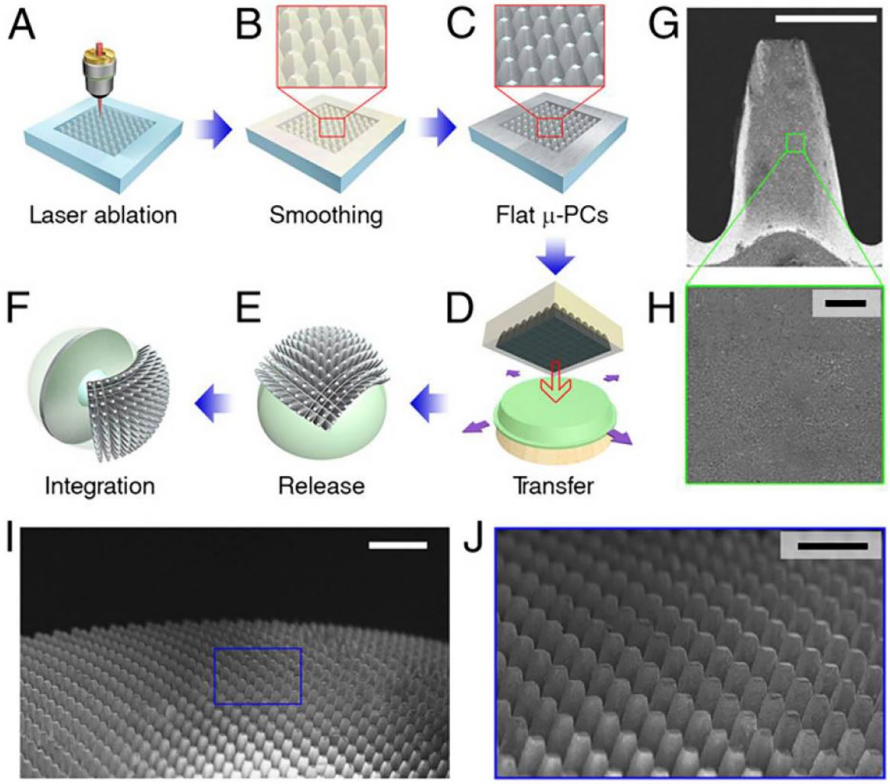
Exploded illustration of the artificial eye, showing the structure of the micro-photocollectors and a possible image sensor implementation across multiple μ-PCs.

the use of dopants within the glass of these micro-structures?

"That's an interesting idea. I haven't thought through about it yet, though. Pretty challenging", says Jiang.

"Whether doped glass could help is questionable. Our mechanism is based on reflection and concentration. Unless doped glass can reduce scattering, it should not matter. Our mechanism is not pumping up light intensity like laser. The incoming light would not trigger that. What you described is more like PMT, which is a different mechanism. That said, it would be really interesting to combine both".

Through further process and geometry optimization, the researchers hope to improve the artificial eye by at least an order of magnitude.



Fabrication process and micrographs of the artificial eye and BPE. (A–F) Schematic illustration of the fabrication procedures. (G and H) SEM images of a μ-PC. (I and J) SEM of the BPE transferred onto a hemispherical PDMS membrane. (Scale bars: G, 50 μm; H, 1 μm; I, 200 μm, and J, 100 μm.) All images courtesy Hongrui Jiang.

TSMC, ARM aim 7nm at data centers

By Rick Merritt

TSMC and ARM announced the next phase of their collaboration on leading-edge semiconductor process technology. Interestingly, they suggest data center and networking chips will be drivers of their work on the 7nm FinFET node.

To date, mobile application processors such as Apple's A series, Qualcomm's Snapdragon and Samsung's Exynos have been among the first SoCs to use new process technologies. Tape outs of mobile chips using 64-bit ARM cores were among the early milestones for 16 and 10nm nodes.

Amid a slowdown in handset growth, the winds appear to be shifting. In a statement released March 15, the two announced "a multi-year agreement to collaborate on a 7nm FinFET process…The new agreement expands the companies' long-standing partnership and advances leading-edge process technologies beyond mobile and into next-generation networks and data centers."

Specifically, ARM said it is preparing a generation of "future ARM technology designed specifically for data centers and network infrastructure and optimized for TSMC 7nm FinFET," according to a quote in the release from Pete Hutton, president of ARM's product group.

To date, ARM's leading edge cores have served a broad array of applications from high-end handset to server SoCs. Late last year, ARM alluded to work on cores for servers and networking and announced libraries specifically for high-performance computing.

ARM and TSMC will use the 7nm collaboration to go beyond past work on test chips to prove a node's readiness. "To better enable our customers design and tape-out optimized SoCs for data centers and network infrastructure, we need to also address design challenges that our mutual customers may be facing," so the duo will hammer out a "design solution [that] is a silicon proof point to demonstrate realistic data center workloads," a spokesman said.

Last year, TSMC said it expects to start making 7nm chips in 2017. That's about the time ARM's initiative to enable server SoCs should start bearing real fruit, said Handel Jones, principal of consulting firm International Business Strategies (Los Gatos, Calif.).

"ARM is very active in trying to get into data centers and 7 nm will be a key technology node for many of these activities… High production volumes are possible in 2019 and 2020," Jones said.

"The server and data center market has strong growth potential in the next few years…[and] customers want an alternative" to Intel's relatively high prices, Jones added, noting Qualcomm and others have announced plans for ARM-based server SoCs.

To date, several companies have announced ARM-based server SoCs, but none have gotten significant traction.

In the press statement, TSMC's vice president of R&D, Cliff Hou, said the 7nm FinFET, process "will deliver more performance improvement at the same power or lower power at the same performance as compared to our 10nm FinFET process node."

Bosch brings traffic applications into the Cloud

By Christoph Hammerschmidt

With its recently announced cloud services, Bosch is addressing multiple regions in the far-flung realm of the Internet of Things. Car users can benefit from some of the applications Bosch is offering.

Cities are threated to be choked by car traffic. According to studies, during the rush hours parking search traffic accounts to one third of all vehicle movements. A system that guides drivers to the next free parking gap would significantly reduce this traffic. Bosch is currently gathering experience with such a system in the Stuttgart metropolitan area, one of Germany's most congested agglomerations with its 2.7 million inhabitants.

For a trial, the company is equipping 15 parking lots in along the S2 and S3 suburban train lines with sensors that determine if a parking space is occupied or free. The data are transmitted into the company's cloud where they are processed, generating an occupancy map with minute-to-minute accuracy. Users can access this map and the related occupancy data through a smartphone app and the website of Stuttgart's urban transportation system.

Car users benefit from the system because they are saving time. Earlier studies have shown that car drivers are more willing to change to public transportation if they know in advance if they would find a free parking spot in their next park-and-ride parking lot. In this pilot project the smallest parking lot has 49 pitches, the largest one 520. The installation of the sensors will be completed in June, 2018.

In another IoT pilot project, Bosch helps truckers and hauliages to book parking spaces for the night. Along the highways in Germany, truck parking lots are hopelessly overcrowded, in particular during night time; theft and robbery has become a problem. With its pilot project, Bosch offers a Secure Truck Parking service. Truckers seeking a parking space transmit their position and a parking space request to the system which in turn finds an unoccupied space. The coordinates are automatically transmitted to the truck's navigation system; booking and accounting are done automatically by the system.

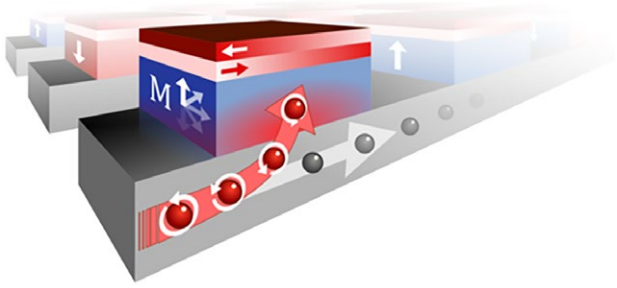
With a third IoT application suggestion, Bosch addresses safety-conscious drivers: an aftermarket Connectivity Control Unit (CCU) is installed in the vehicle that and connected to the on-board diagnosis socket. It accesses data such as longitudinal and lateral acceleration, speed, and time of the day. Through a built-in SIM card, the CCU sends these data in encrypted form to the insurance company. The insurer can use these data to create a risk profile; for drivers who are driving proactively they can offer a discount.

MRAM breakthrough looms

By R. Colin Johnson

Everybody in the memory business is trying to build a nonvolatile memory that is as fast as static random access memory (SRAM), as dense as flash and as cheap as read-only-memory (ROM). The problems with this "universal" memory (that could replace all others) has already been solved by magnetic random access memories—according to those making MRAM.

Unfortunately, the optimization step to actually make nonvolatile MRAM faster, denser and cheaper—that MRAM makers keep promising—always seems to be three years away. Now independent researchers at Eindhoven University of Technology (TU/e, The Netherlands) claim to have solved the fast, dense and cheap problem with a novel new approach called "field-free magnetization reversal by spin-Hall effect and exchange bias"—or "current bending" for short.



Magnetic bits are quickly switched by bending electrons with the low-current pulses to attain the correct spin, while a special anti-ferromagnetic material makes the process cheap. (Source: Arno van den Brink)

"The current density required to write magnetic bits becomes prohibitively high as bit dimensions are reduced," said the TU/e team of physicists led by professor Henk Swagten in their Nature paper. "By interfacing the perpendicularly magnetized layer with an anti-ferromagnetic material, creating an in-plane exchange bias (EB) along the current flow direction, we demonstrate a spin-Hall effect driven magnetization reversal using only the intrinsic in-plane magnetic field caused by this EB." In other words, what they call "current bending" seems to solve the fast, dense and cheap problem of nonvolatile MRAM.

If you are familiar with MRAMs, then you already know that they store ones and zeros on the up or down spin of electrons, rather than accumulating or dissipating charge through a current-hogging tunnel barrier, thereby intrinsically saving energy to the max by what is called the "spin-Hall effect." Still they required spin-encoded electrons to be run through the ferromagnetic material to flip a bit, which did not scale well. In a nutshell, Swagten's team runs a tiny current pulse under a bit to flip its spin—hence the "current bending" moniker—which is not only more energy efficient, but scales like Moore's Law.
The technique is also super-fast, according to the team, but still needed to be optimized for cost. The researchers claim to have solved that last problem by capping a layer of inexpensive anti-ferromagnetic material atop the bit cells, effectively "freezing" their magnetic field to meet the fast, dense and cheap goals.

Pitching one AI solution against next

By Julien Happich

According to Artificial Intelligence software solutions provider Dato, apps of the future will all run a form of machine learning or another to better serve their users. One of the company's early customers, LodgIQ plans to revamp today's hospitality industry with smarter real-time pricing strategies based on the analysis of big data. Founded last December, the New-York based startup was quick to convince investors, securing $5 million in funding from investors Highgate Ventures and Trilantic Partner while signing its first customer, Highgate Hotels.

The company has just launched its first products, LodgIQ RM and LodgIQ Mobile RM (for Revenue Management). The LodgIQ RM platform incorporates machine learning and artificial intelligence to adapt to evolving demand patterns in real-time. One application could be to help hotel managers adjust their commercial and pricing strategies continuously, based on multiple factors such as flights patterns, weather forecast, city events (trade-fairs, concerts, sporting events), online reviews, or anything that may affect travellers' destinations and booking patterns.

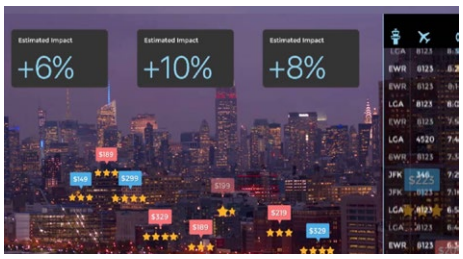
Talking to *EETimes Europe*, LodgIQ's CTO Somnath Banerjee explained his ambition to apply modern scientific mathematical techniques to price hotel rooms.

As a hotel manager, the tool could help you find out dynamically who are your savviest competitors in particular segments, or within a given distance.

"We use historical data, but also large data sets from flight reservations, weather forecast, city-events, or even text-based hotel reviews, and quantify their impact on reservation patterns. We use machine learning to identify patterns in data that we can use for our predictions in order to suggest the best room prices for a given market condition".

Today, hotel managers typically list out their competitors' prices manually, but this would no longer be possible with dynamic pricing, and they may not optimise their room prices based on statistically accurate demand.

"There are many things in life that are subjective, for example online hotel reviews are very important, but they are often text-based. We want to take them and run AI across them to mathematically quantify their impact on revenue, putting an objective number on them so hotel managers can find out what their hotel's real score is".



The idea is to measure the exact correlation between improved reviews and increased revenues, and how these reviews might be improved (the key actions at staff or service-level). Today, this is very nebulous affair, but machine learning could help hotel managers better understand what impacts their business and how they can optimise their pricing strategies accordingly.

"There was first pen and paper, then electronic spreadsheets and today web-based management, but the future is all about machine learning", Banerjee says.

But what will happen when all hotel room pricings will be automated, dynamically updated by competing AI solutions scouring not only big data but also closely watching their competitor's dynamic pricing routines? Wouldn't that inevitably circle back to equalize room prices at their lowest manually set threshold values?

"This scenario is a utopia where every hotel manager would have the same skills and operate the same hotel", dismisses Banerjee.

In reality, whilst machines can make recommendations, they will also foster creativity in terms of pricing strategies. Hotel managers will differentiate their pricing schemes based on how they match their offers with the particular data patterns they see which affect their hotel differently. Integrating AI into their revenue-management tools will help them create that differentiating edge.

"For the next 30 years, the future is all Maths and Statistics" concludes the CTO.

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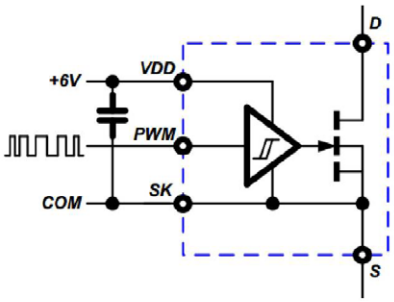
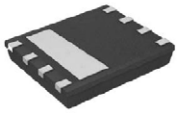
All GaN driver integration takes power switching to 40MHz

By Julien Happich

Founded in 2013, Californian startup Navitas has unveiled its roadmap for Gallium Nitride (GaN) power ICs based on its proprietary AllGaN monolithically-integrated 650V platform. With the monolithic integration of GaN power FETs with drive and logic, the company claims 10x to 100x higher running frequencies than existing silicon circuits, setting new benchmarks in power density, energy efficiency and system cost.





The AllGaN platform was presented at the Applied Power Electronics Conference (APEC) by the company's CTO / COO & Co-Founder, Dan Kinzer, in a keynote titled "Breaking Speed Limits with GaN Power ICs".

EETimes Europe caught up with Navitas' Vice President of Sales & Marketing, Stephen Oliver to learn more about the company's ambitions.

About Navitas' technology breakthrough, Oliver says, "Today, if you want to use a GaN FET, you need to add a control IC and a silicon driver, that's a three-chip solution. Using a lateral hetero-epitaxy structure, we are able to integrate the driver directly on the GaN FET, which we can run at up to 40MHz".

The good thing is that by integrating drive and logic functions laterally, the company can use large-diameter GaN on Si wafers.

"If you tried to integrate the logic vertically, GaN on GaN, then you would be limited to very small and expensive 3-inch wafers", Oliver explains.

This makes Navitas ready to deliver high volumes using existing equipment from existing OSAT companies. Indeed, the startup plans to follow a fabless business model, it will sell devices but it could well license its IP too.

From the start, company Co-Founder Dan Kinzer had clear ideas on how to take GaN to its full potential.

"You have to remember that Kinzer is a very experienced guy, he was the process guy at IR who took the HEXFET from blueprint to a real product". We started up with a basic FET structure licensed from a US research lab and developed our own process design kit with added lateral structures", commented Oliver.

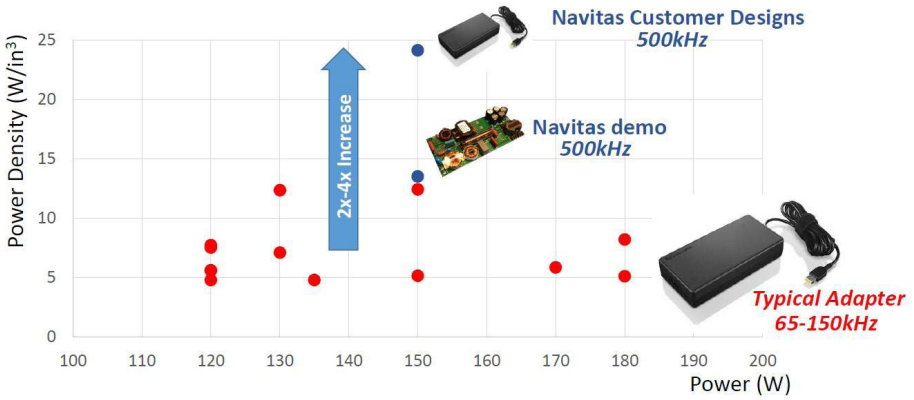
"We'll start our product roadmap with single FETs with a monolithically integrated driver to go after applications from AC to high voltage DC in a high performance QFN package only 5x6mm, then we'll move to multiple FET ICs with multiple drivers and added logic functions such as hysteretic digital inputs, voltage regulation or ESD protection", Oliver said, mentioning that his company has been sampling its first products at the end of 2014.

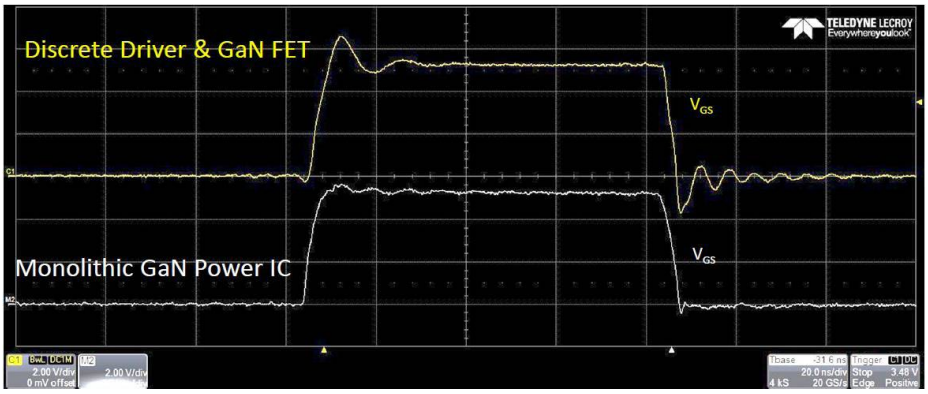
"Our first range of devices will target applications from 300 to 500W, anything from chargers to TV power supplies. In 2015, we engaged with multiple prototyping customers, their first reaction was that our GaN FETs behaved like an ideal switch.

It only takes a very small current to turn on the signal (with a prop delay as low as 5ns) and deliver the power, the waveform on the oscilloscope looks like an ideal simulation, with no overshoot or spike, nor oscillations".

According to the company's presentation material, while typical adapters run at 65 to 150kHz and achieve a power density of about 5 to 12W/in^3, Navitas' first demo achieved a power density of 13.5W/in^3 when running at 500kHz, something customers aim to push to 20-25W/in^3.

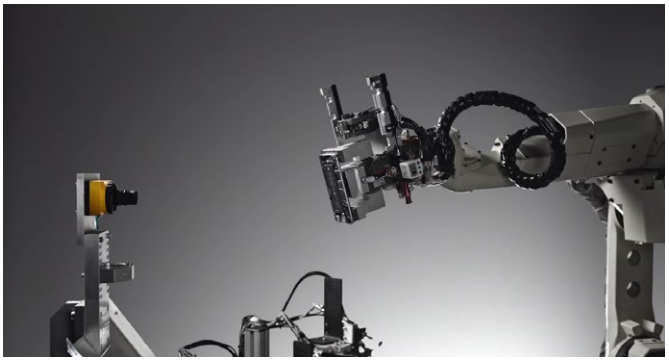
Navitas is expecting its first official product release next summer.





Apple takes a recycling step

By Peter Clarke



Apple is to be applauded for creating a system to recover at least some of the resources it has gone to such trouble to assemble in its iPhones. Previously these planetary resources were to a great extent, locked into the iPhone – as they are in billions of pieces of electronics equipment. But now comes Liam, a system that deconstructs the iPhone at the end of its life to identify parts and remove them so that, where possible, they can be reused. This extends to the extraction of precious metals such as cobalt, lithium, gold, copper, platinum and silver from batteries, cameras and PCBs.

The system has been three years in development according to Charissa Rujanavech, who works in environmental initiatives at Apple.

I don't know how effective Liam is and it may be that Apple is doing a little bit of recycling and trying to derive a lot of marketing benefit from that effort.

Is there a Liam for the iPad and for Apple computers? What if Apple were to share this system, through the likes of equipment assembler Foxconn, with the entire consumer equipment industry.

But at least Liam for the iPhone is a step in the right direction and its shows that Apple understands that consumerism must learn to coexist with environmental considerations. This was something a certain Qualcomm executive lacked back in 2013 when he was asked about recycling by a young student at the IMEC Technology Forum in 2013.

The Qualcomm executive had been more or less crowing that the two-year equipment cycle – born of Moore's Law and handed down to the public by the mobile network operators – was a license for Qualcomm to print money.

But when asked what the company had done about recycling the executive seemed to be at a loss to understand the question. It was left to the questioner to be more specific about what he meant. What is Qualcomm doing to design phones and chips so that component elements and materials are more easily recyclable, and thus mitigate the waste of throwing away a phone every other year?

Apple at least now has an answer to that question.

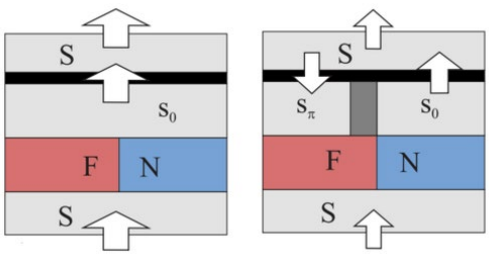
Russian researchers propose 100x faster memory

By Peter Clarke

A group of Russian scientists have developed a control system for superconducting memory cells that take less than a nanosecond to read or write, hundreds of times faster than similar memories in use today.

The scientists, from the Moscow Institute of Physics and Technology (MIPT) and from Moscow State Univeristy, have reported their work in an article published in the journal Applied Physics Letters.

The work is a theoretical study that predicts the existence of a bistable state in a complex superconducting Josephson Junction device. An implementation of the device may require supercooling for operation making it less than practical for some applications.



A team led by Alexander Golubov, the head of MIPT's Laboratory of Quantum Topological Phenomena in Superconducting Systems, have proposed a memory cell based on quantum effects in a type of Josephson Junction, a superconductor-dielectric-superconductor sandwich, in which one side of the junction includes a combination of ferromagnet and normal metal. This should be bistable with switching between the two states (the one and the zero) effected by an electric current injected laterally into the structure. The state of the system can be non-destructively read by an electric current flowing across the junction.

Superconducting currents when reading various states of the memory cell. The greater current the larger arrow. Source: MIPT.

Read and write operations are predicted to take a few hundreds of picoseconds depending on the materials and the geometry of the particular system.

"In addition, our method requires only one ferromagnetic layer, which means that it can be adapted to so-called single flux quantum logic circuits, and this means that there will be no need to create an entirely new architecture for a processor. A computer based on single flux quantum logic can have a clock speed of hundreds of gigahertz, and its power consumption will be dozens of times lower," said Golubov, in a statement.

Why Audi's zFAS is a blueprint for next-gen domain architectures

By Christoph Hammerschmidt

In Audi's future car generations, a central computer assumes many if not all of the various tasks associated to the diversity of driver assistance systems. The zFAS (central driver assistance controller) greatly reduces the number of electronic control units – a concept that will set a precedent for other carmakers and for future domain architectures.

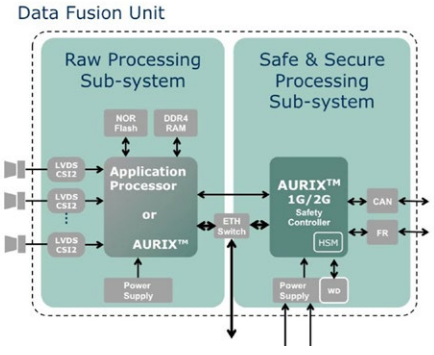
The zFAS, scheduled to enter series production in the next version of the A8 top-class sedan due end of 2017, unites multiple computing tasks on one powerful main board. Its most demanding role is sensor fusion. Here, the signals from multiple sensors like stereo cameras, radar, multi-axis acceleration sensors and, if applicable, lidar sensors are merged and transformed into a 360-degree digital environmental model which in turn is used by all the driver assistance systems including those responsible for autonomous driving to compute their respective action.

"We need the zFAS for piloted driving in series," an Audi spokesperson acknowledges.

Audi's zFAS central driver assistance controller.

In the zFAS therefore multiple microprocessors and microcontrollers share the workload. Basically, an application processor handles the compute-intensive image processing and low-level data fusion tasks; the host processor is responsible for the safety-critical aspects like object fusion, decision making and vehicle communication as shown in the block diagram.

It is known that Audi has a special relationship with Nvidia and therefore uses processors like the Tegra K1 for most tasks associated to graphical computing. But since the various sensors in the vehicle – front cameras, surround cameras radar etc – generate such a huge amount of data, the carmaker's design engineers have chosen to employ two processors with the task of processing the sensor data – a Tegra K1 and a device from Mobileye, the EyeQ3 SoC. The Tegra is dedicated to processing the data from the four surround cameras; the data is used to assist the driver during parking. In the current version of the zFAS that will enter series production, the more time-critical data from the stereo front camera are fed to the EyeQ3. In addition, it will handle the data from the driver monitoring camera, another requirement for piloted driving.



More computing power than all ECUs in today's cars combined: Generic view of a domain controller for Driver Assistance Systems that make use of sensor data fusion. Source: Infineon

The safety-relevant portion of the action is handled by an Aurix multicore microcontroller from Infineon. "You need to differentiate between the computational tasks associated to the graphical procedures and the really safety-critical decision making," explains Thomas Boehm, Senior Director, Chassis and Safety Microcontrollers at chipmaker Infineon.

"For decision-making and communications, the real-time requirements are significantly higher." These tasks have to meet high functional safety standards such as ISO 26262, and the Aurix architecture therefore provides lockstep mechanisms – two identical cores that perform the same computational tasks; if the results do not match, a safety interrupt stops the system.

The communication between the application processor and the host processor occurs across a high-performance Ethernet switch on the PCB, implemented in an Altera Cyclone 5 FPGA. Additionally, this chip is responsible for the central timing and functions on the board, "a very important aspect", the Audi spokesperson notes.

The Ethernet bus within the zFAS board is not the same Ethernet we it from our office computers, but instead a species of deterministic Ethernet developed by Austrian technology company TTTech. This company also developed the middleware layer that enables the platform to run multiple virtual machines in a safe and secure manner. The middleware is compatible to the Autosar, the automotive standard software framework, explains Marc Lang, Director Sales & Marketing Automotive at TTTech. "The virtual machines with their applications are hermetically separated against each other to make sure that they have no mutual interaction", Lang says. "The communication between tasks runs across the middleware layer."

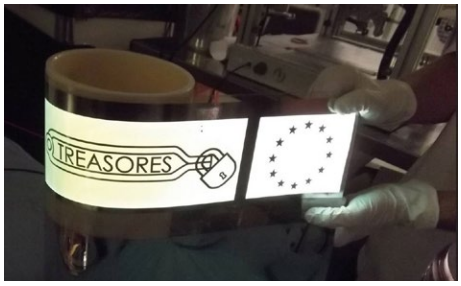
Audi's zFAS design has already stimulated similar efforts across the automotive industry, Lang and Boehm acknowledge unanimously. Driven by the desire of carmakers to reduce the complexity of automotive control electronics - today, already a medium-sized vehicles run some 80 separate electronic control units, each one for a single task – OEMs transplant the basic architecture of the zFAS to other real-time critical domains like chassis control.

The computing power and functional safety of this architecture enables innovative functions like torque vectoring or four-wheel steering, Lang says. Aurix is not the only architecture deployed in this environment; Lang says that he also has seen implementations with Renesas or NXP (formerly Freescale) processors. Nevertheless, Infineon holds a strong position in this field. "We know several OEMs that will bring their Aurix-based systems to the market in 2016", says Boehm. In particular the usual suspects among the European premium OEMs are on the starting blocks. Including Audi itself: the carmaker already has plans to apply the zFAS approach to other domains beyond driver assistance. In the future, there will be only eight domain controllers instead of dozens of dedicated ECUs", the Audi spokesperson quotes E/E development manager Rick Hudy.

European research delivers on OLEDs

By Julien Happich

Funded with 9 million Euro from the European Commission and an additional 6 million Euros from the project partners, the TREASORES project (Transparent Electrodes for Large Area Large Scale Production of Organic Optoelectronic Devices) yielded promising results that could boost the adoption of organic solar cells and OLED lighting panels.



Initiated in November 2012 and uniting the efforts of nine companies with six research institutes from five European countries, the project resulted in seven patent applications relating to the production of new transparent electrode and barrier materials for use in the next generation of flexible optoelectronics.

Sometimes using carbon nanotubes, metal fibres or thin silver, the flexible electrodes have been tested with several types of optoelectronic devices using rolls of over 100 meters in length, and found to be especially suitable for next-generation light sources and solar cells.

The roll of OLED light sources with the project logo (as per the top photo) was made using roll-to-roll techniques at Fraunhofer Institute for Organic Electronics, Electron Beam and Plasma Technology FEP on a thin silver electrode developed within the project by Rowo Coating GmbH.

Such processing techniques promise to make light sources and solar cells much cheaper in future, but require flexible and transparent electrodes and water impermeable barriers, which were also investigated and developed by the TREASORES project.

According to Fraunhofer FEP, the electrodes from the project are technically at least as good as those currently used (made from indium tin oxide, ITO) but will be cheaper to manufacture and do not rely on the import of indium.

In the course of the project, new test methods were developed by the National Physical Laboratory in the UK to make sure that the electrodes would still work after being repeatedly bent – a test that may become a standard in the field.

A further outcome of the project has been the development, testing and production scale-up of new approaches to transparent barrier foils (plastic layers that prevent oxygen and water vapour from reaching the sensitive organic electronic devices). By combining the production of barriers with electrodes (instead of using two separate plastic substrates), the project has shown that production costs can be further reduced and devices made thinner and more flexible.

The main challenge the project had to face was to make the barrier and electrode foils extremely flat, smooth and clean. Optoelectronic devices have active layers of only a few hundred nanometres, and even small surface irregularities or invisibly tiny dust particles can ruin the device yield or lead to uneven illumination and short lifetimes.

New devices using the patented electrodes and film barriers are expected to see the light in 2016.

Led by Frank Nüesch from the Swiss Federal Laboratories for Materials Science and Technology (Empa), the TREASORES project's partners included the Technical University of Dresden; Germany, the Fraunhofer FEP, Fraunhofer ISC, Fraunhofer IVV and Fraunhofer ISE, Germany; the University of Valencia, Spain; Aalto University, Finland; CIC Nanogune, Spain; NPL Management Ltd., United Kingdom; Osram GmbH, Germany; Canatu Oy, Finland; Amanuensis GmbH, Switzerland; Sefar AG, Switzerland; Amcor Flexibles, Switzerland and Germany; Rowo Coating GmbH, Germany; Eight19 Ltd., United Kingdom and Quantis Sàrl, Switzerland.

Lawrence Livermore to deploy IBM neural network computer

By Peter Clarke

The Lawrence Livermore National Laboratory has announced it will take delivery of a supercomputer based on the TrueNorth neural networking chip developed by IBM.

The computer will be scalable but based on 16 TrueNorth chips will process information using the equivalent of 16 million neurons and 4 billion synapses while consuming 2.5 watts, the laboratory said. The computer will be used for object classification, pattern recognition and integrated sensory processing.

Built on Samsung's 28nm process technology TrueNorth comprises 5.4 billion transistors in a 4.3 square centimeter die. It contains one million neurons and 256 million synapses implemented by an on-chip 64 by 64 mesh array of 4,096 neurosynaptic cores. Each core integrates memory, computation, and communication, and operates in an event-driven, parallel, and fault-tolerant fashion.

TrueNorth was originally developed under the auspices of the Defense Advanced Research Projects Agency's (DARPA) Systems of Neuromorphic Adaptive Plastic Scalable Electronics (SyNAPSE) program, in collaboration with Cornell University.

Under terms of the $1 million contract, LLNL will receive a 16-chip TrueNorth system representing a total of 16 million neurons and 4 billion synapses. LLNL also will receive an end-to-end ecosystem to create and program energy-efficient machines that mimic the brain's abilities for perception, action and cognition.

The ecosystem consists of a simulator; a programming language; an integrated programming environment; a library of algorithms as well as applications; firmware; tools for composing neural networks for deep learning; a teaching curriculum; and cloud enablement.

Modular and mobile photovoltaics on wheels

By Julien Happich

Dutch startup Solar Application Lab has designed a prototype solar e-bicycle that integrates multiple solar panels on its front wheel, enough to recharge the e-bike's battery over the course of the day.

Sporting a 250W front-wheel integrated electrical engine, a 400W 36V 11A battery and 60 mini solar panels which provide the S-bike with an average of 35 to 40Wh per hour during daytime under the fairly clouded Dutch skies, the prototype was proving enough for the startup to secure strong partnerships with well-established bicycle manufacturers.

The first prototype was designed based on mono crystalline cell technology but the company is working in close cooperation with the Delft University of Technology to develop a second prototype based on amorphous silicon, hopefully ready within the next 6 to 12 months.

Although organic flexible photovoltaics are on its radar, the startup sees them as a longer term prospect, knowing that its energy harvesting architecture is cell-technology agnostic and could accommodate any new photovoltaic configuration.

Solar Application Lab's first prototype sports 60 mini solar panels on its front wheel and a hub-mounted electric powertrain.

To make the most of each individual panel, the S-bike relies on a patented nano-inverter architecture which the company says makes the cluster of cells more efficient and ensures a stable power output, even under partial shading or at varying light angles.

Having proven the concept, Solar Application Lab hopes to co-develop a solar e-bike with partners from the cycle industry, to whom it would then license the nano-inverter IP.

"In fact, the Solar Cycle is a vehicle for our IP", told us Marc Peters, the company's Founder and Managing Director.

"We couldn't work with existing micro-inverters from the photovoltaics industry, those would have been an overkill for our application. So we had to build our own architecture from discrete components" he explained.

"Our nano-inverter can work with any type of solar cell in any cluster configuration, on a small scale" he continued. The Solar Cycle is a starter, aimed at the booming e-bike market.

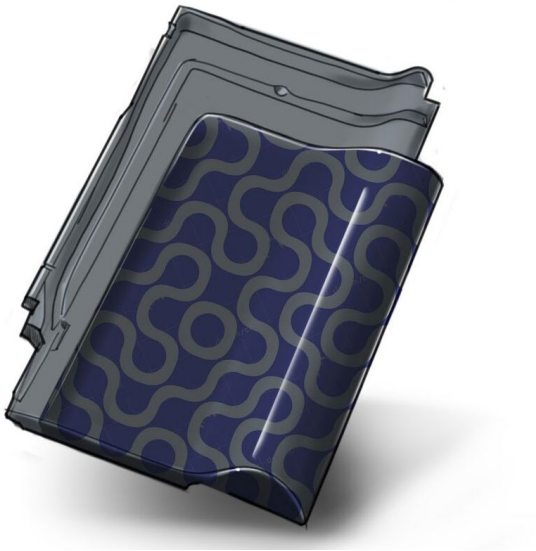
If it becomes a success, maybe the company will have the multi-million euros budget to turn its IP into silicon.

"We want to design an ASIC for it, most definitely" said Peters, hinting at the 130 or 90nm nodes, "or maybe two or three product versions to cater for 80 to 90% of the market for small scale modular photovoltaics". For example, derivative products enabled by such an all-silicon nano-inverter could include unique photovoltaic tiles designed to be laid out in clusters of any size.

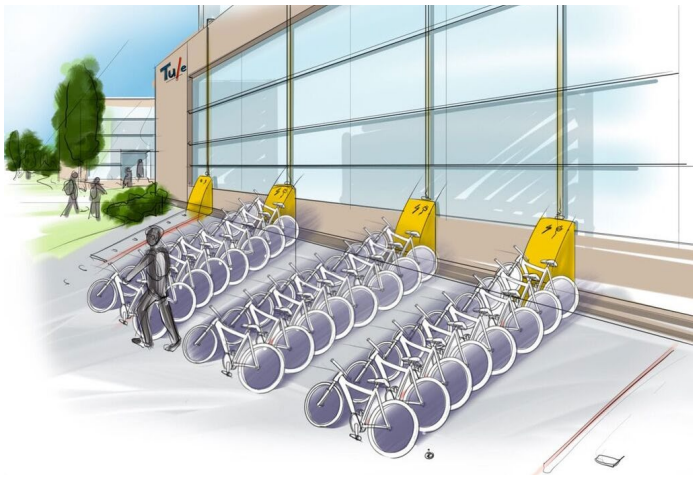
In volume production, a chip solution could take the costs down dramatically compared to today's discrete board designs, estimates Peters, it would also help the company diversify its market, say to design readily connectable photovoltaic tiles.

Solar Application Lab has received approximately 250,000 euros of seed funding (the company was created in July 2014), and is currently setting up a collaboration programme of 1.2 million euros with undisclosed companies willing to co-develop a commercial product.

"The prospect investors aren't specifically linked to the bike industry", clarifies Peters, "because even though the bike application is linked to the ASIC business case, the two don't



A nano-inverter ASIC could take Solar Application Lab well beyond the e-bike market, managing unique solar tile designs.



e-bikes could contribute to a city's smart power grid, when plugged into dedicated infrastructure.

necessarily have the same investment scopes. Solar Application Lab needs to raise approximately 400 to 500k for the next two years".

The Solar Cycle as an affordable and green mean of transportation is only one part of the story, though. Peters wants to exploit the modular and mobile solar concept further, by making the solar panels removable, maybe to be affixed to a building's wall upon arrival.

Or alternatively, when not in use, the e-bikes could contribute to a city's smart power grid, when plugged into dedicated infrastructure (akin to electric cars today).

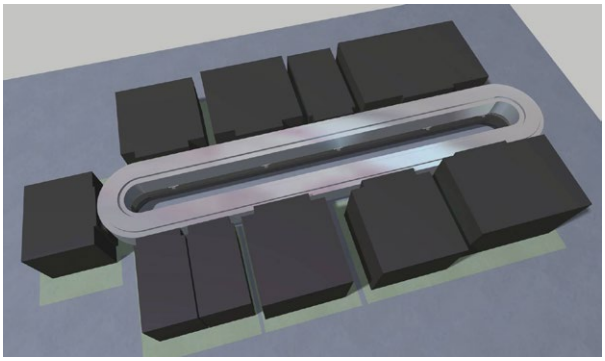
Peters is planning to launch a crowdfunding campaign this summer. He hopes the campaign's story telling will help mobilize not only early adopters but also incubators and policy makers from cities with strong ambitions to pioneer green and smart infrastructures.

Flexible electronics scale up to billions with fab-in-a-box

By Julien Happich

Flexible electronics solution provider PragmatIC has completed a detailed design study validating its FlexLogIC "fab-in-a-box" concept for production scale-up of flexible integrated circuits (flexICs).

The first FlexLogIC system to be commissioned from Deutch contract manufacturing partner VDL Enabling Technologies Group (VDL ETG) and expected in 2017, will transfer PragmatIC's proven end-to-end flexIC production process into a self-contained, fully automated, modular design, with capacity for billions of flexICs at a capital cost between 100 and 1000 times lower than a silicon fab.

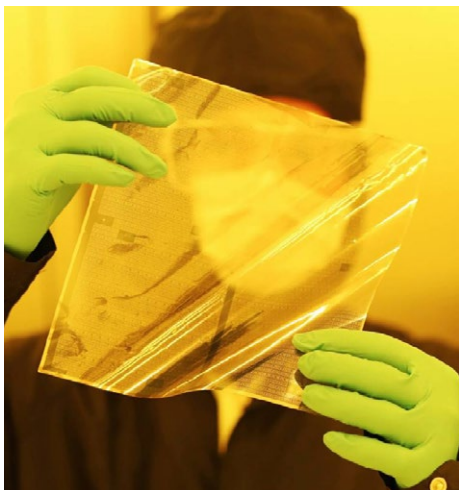


Concept illustration of the FlexLogIC system.

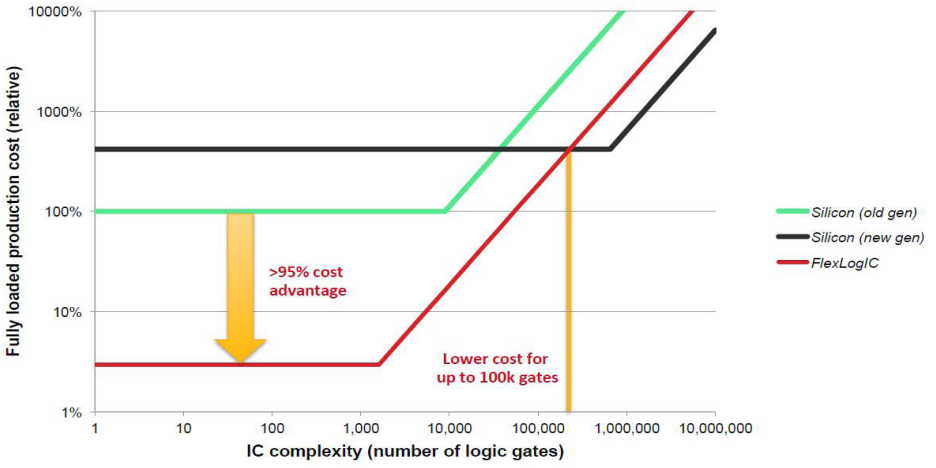
"The initial system will be focused primarily on scale-up of production based on our current design rules, however the architecture is easily adapted with only minor changes for future nodes. Throughput is in the billion of flexICs per annum (depending on functionality etc). The system includes fully automated software control. We are also developing IP libraries including reference product designs based on our existing standard cell libraries, but would expect to leverage our partner relationships to ensure a complete ecosystem (e.g. ARM)", told us PragmatIC's Chief Executive Officer, Scott White.

Although the first system will be used in-house by PragmatIC to scale up production for its existing customers, the company expects that as certain products reach maturity and mass-market volumes, its business model could evolve to include sales of FlexLogIC systems (along with a technology licence) to customers/partners for their own in-line production.

The CEO pointed that already five customers had showed their interest in buying a FlexLogIC system for their own production purposes.



A sheet of flexible circuits on plastic.



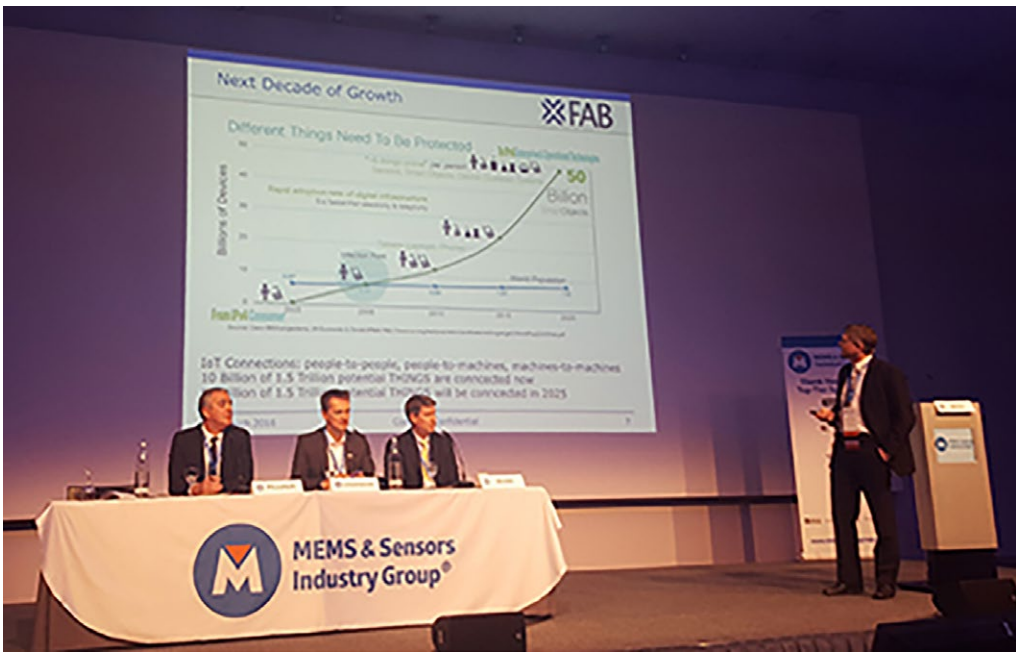
NB, analysis assumes footprint is limited by complexity not I/O pads (more pads would increase inflection & crossover point) - (source PragmatIC).

Panel ponders MEMS roadmaps, a Moore's Law of MEMS

By Peter Clarke

Could oversupply be coming to MEMS? A panel at the MEMS & Sensors Technical Congress held in Munich, Germany, this month was asked to find solutions to challenges to the growth of the MEMS industry over the next decade but raised more questions than answers.

The panel ended up more or less back at the one fact that has dominated MEMS and has both enabled it and hindered it. The first law of MEMS is: "One product, one process, one package." But the panel also highlighted the potential risk of MEMS oversupply either from over-exuberant established manufacturers or possibly from Chinese entrants into the field.



From left to right: Pilloux, Sonnemann, Monk and Merz consider how many MEMS components each industrialized person will use.

The panel pointed out that the 3Ps rule of MEMS is a double-edged sword; it favors customization and fragmentation rather than standardization and scaling but it has created a rich garden of exotic sensors and actuators based on a wide variety of transduction principles.

However, the panel discussion did raise the possibility of an incipient equivalent to Moore's Law based around packaging and how the awareness amongst the members of industry bodies such as MEMS & Sensors Industry Group, organizer of the conference, could help drive standardization.

The session was moderated by Peter Merz, MEMS business unit manager at X-Fab Silicon Foundries AG and the panel comprised Dave Monk, general manager of the motion sensors business unit at NXP Semiconductor, Markus Sonnemann, vice president of engineering at Robert Bosch GmbH and Yannick Pilloux, business development manager for MEMS at manufacturing equipment supplier PlasmaTherm LLC.

Their task was to enable another decade of MEMS industry growth, if they could.

The Internet of Things (IoT) would certainly appear to be boon to MEMS vendors with the enormous volumes of simple machines that are expected to be connected to the Internet in 2025, 50 billion devices according to Cisco.

Projections showed by Merz put the demand at 12 MEMS per person across the globe in 2025 or 105 MEMS per "industrialized" person with the majority shared between the automobile, the public environment, in the home and in wearable/mobile equipment.

But to achieve such volumes at average selling prices (ASPs) that are affordable to the public and motivating to industry players appears difficult. Not least, the panel agreed, because the MEMS sector does not scale the same way that CMOS and digital semiconductors have done.

The long trajectory for process development, a decade or more, has left strategic cooperation as an exceptional practice in the sector. NXP's Monk said: "The supply chain is adequate but not enabling. Standard processes are still fairly limited."

Bosch's Sonnemann added: "We are hopeful of IoT but we don't see the volume yet. The barriers are a lack of interface standards and the many RF protocols, security and software. We've made a start on software with sensor fusion but it is not yet clear how much software MEMS providers must offer with the hardware."

Although not mentioned in the discussion there is also the risk that MEMS vendors will be expected to provide software for free as part of the sale of piece parts priced at a few cents. The "free software" phenomenon has already struck at suppliers of digital chips.

A speaker from the floor with the US National Institute of Standards and Technology (NIST) pointed out that the semiconductor industry has come to the end of its roadmap as organized by the International Technology Roadmap for Semiconductors (ITRS), but that it had served semiconductors well for 40 years.

"Perhaps a MEMS & Sensors Industry Group roadmap is needed," he asked. The debate continued on the floor as to whether such roadmaps generate impetus or merely orchestrate progress that is driven from elsewhere.

The panelists noted that the Trillion Sensors initiative created by serial MEMS entrepreneur Janusz Bryzek and now administered by the MEMS & Sensors Industry Group is the closest the MEMS and sensors sector has to a roadmap.

Bryzek was moved to create the TSensors initiative after reading the book "Abundance" authored by Peter Diamandis and Steven Kotler. That book looks at exponentially advancing technologies – such as semiconductors, smartphones – and their markets and extrapolates that it will soon be possible to meet the basic needs of every man, woman, and child on the planet (see www.abundancethebook.com).

However, an audience member took a darker view when he suggested that the survival of the human race may depend on the TSensors initiative as the means to head-off an Armageddon that will otherwise be created by climate change and water shortages.

"This may obviate the need for privacy and security as we move from a "wants" based society to a "needs" based one," the audience member said.

A Moore's Law of MEMS?

Coming back to the idea of a Moore's Law for MEMS, Monk pointed out that since 2006 the physical size of the three-axis accelerometer component has decreased by 50 percent every 18 months and it is driven by economics just as the original Moore's law was. "The economics of scale will be solved by the supply chain," he said.

While Monk's observation was at the packaging level it is also notable that the tiny area taken up by MEMS dies makes it hard for the sector to move manufacturing up from 6-inch and 200mm-diameter wafers.

Bosch's Sonnemann said he could see no need for moving production of MEMS to production on 300mm-diameter wafers any time soon but that roll-to-roll production of low-cost, low-performance of some sensors had attractions.

"In five years silicon will still be the number on MEMS technology. But who will have come from China? That will be the interesting question."

X-Fab's Merz was left to wrap up a panel session that had solved no problems but provided plenty of food for thought, especially in the area of roadmaps and standardization.

"In five years we may have overcapacity in MEMS. I hope not and meanwhile I hope we work on a roadmap and standardization," he concluded.

MEMS gravimeter takes underground mapping to the masses

By Julien Happich

Using a proprietary asymmetric cantilever design, researchers from the University of Glasgow have designed a portable MEMS-based gravimeter boasting the smallest resonant frequency ever reported for a MEMS device together with unprecedented stability.

With its resonant frequency of 2.3Hz, an acceleration sensitivity of 40μGal $Hz^{-1/2}$ and a stability guaranteed for days or even weeks thanks to very accurate servo control loops that maintain the system's temperature to within 1mK, the device can be used to monitor minute variations in gravity over long time spans, making it applicable to many fields of geology and underground exploration.

In a paper titled 'Measurement of the Earth tides with a MEMS gravimeter' published in Nature, the researchers detail the unique geometry of their 15x15mm MEMS die featuring an anti-spring flexure pair at the bottom (constraining the motion of the proof mass) and a curved cantilever at the top.

The proof mass motion is measured using an optical shadow sensor (a photodiode placed on one side measures the proof mass' shadow variations as the MEMS is illuminated from the other side by a LED – see figure 1).

This sensor setup achieves a high sensitivity, equating to an acceleration noise floor of under 10μGal at the sampling frequency of 0.03Hz, while allowing a large dynamic range of up to 50mm, explain the researchers. Key to the MEMS' long term stability is the precise temperature control mechanism, achieved through the use of four small platinum resistors (one on the outer frame of the MEMS and three placed equidistantly around the copper shield of the full device).

Limiting temperature variations to within 1mK is necessary to stabilize the MEMS' mechanical characteristics (through minimized thermal expansion fluctuations) and spring constant. A change in temperature of 1mK would give an uncertainty in the gravity reading of about 25μGal, the paper explains.

Although this MEMS-based gravimeter is a technological feat, in terms of compactness and sensitivity, it would look rather bulky compared to the typical MEMS accelerometers found

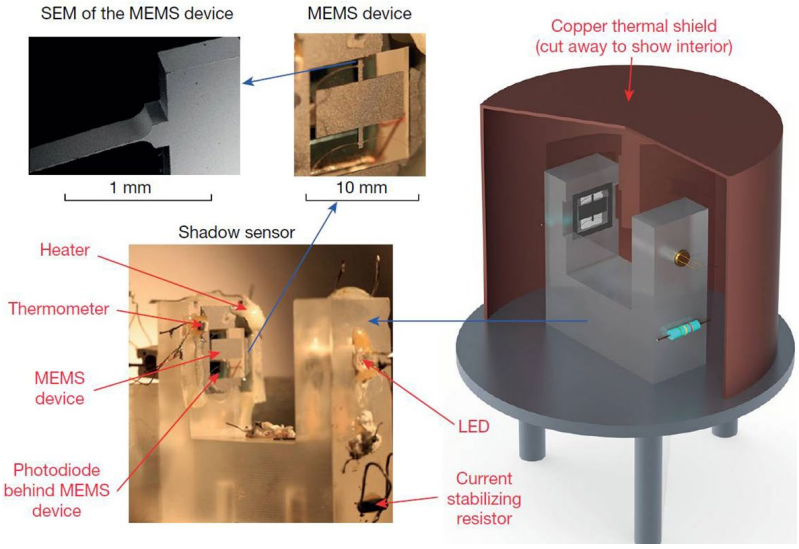


Fig. 1: Both the MEMS device and the shadow sensor sit on an aluminium plate and are encased in a copper thermal shield. At the top left is a photograph and scanning electron microscope (SEM) image (copyright for both images R.P.M., 2015) of the MEMS device. At the bottom left is a photograph of the MEMS device mounted on the optical shadow sensor with glue holding the heater and thermometer in place (copyright G.D.H., 2015).

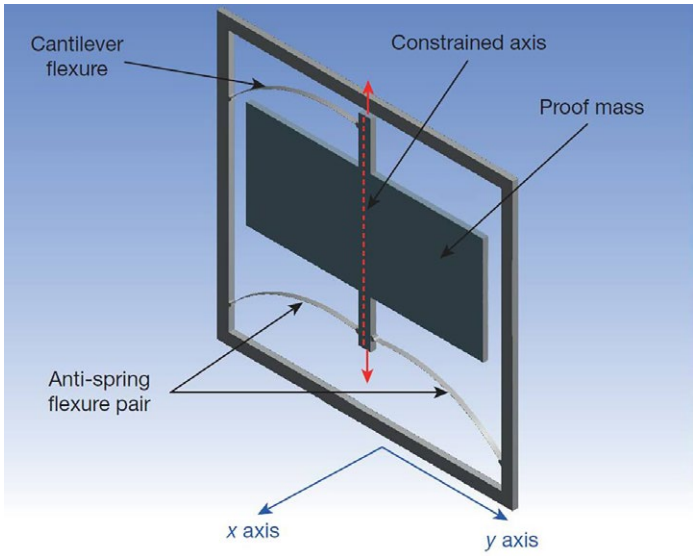


Fig. 2: The MEMS gravimeter is suspended from three flexures: an anti-spring pair at the bottom and a curved cantilever at the top.

in consumer electronics (these are in fact much more rigidly designed, with smaller proof mass to cantilever aspect ratios).

But as co-author Dr Richard Middlemiss explained, the sensitivity and the softness of the springs necessary for a very low resonant frequency are only achieved thanks to very high aspect ratios in the design.

"All the flexures are only 7μm wide but 250μm deep, etched vertically through the silicon die", Middlemiss told *EETimes Europe*.

"There is scope to miniaturize the full MEMS die and we could probably design a similar structure with flexure thinned down to 0.5μm while still keeping a clean high aspect ratio using photolithography. We've not got to that point yet with our models, but this is certainly something we'd like to explore"

Middlemiss says that although the gravimeter prototype is very much an R&D experiment at this stage, it could certainly be further integrated on silicon, with on-chip sensors, thermal control and better integrated optical detection.

"The Wee-g system will not displace accelerometers any time soon", admits Middlemiss when asked if such MEMS-based gravimeters could one day leverage crowdsourcing for gravity mapping, "but if we were to offer a solution only a few cubic centimetres in volume, then we could make this relative gravimeter widely accessible for new fields of application where money is often scarce".

Today's commercial solutions with that type of sensitivity typically sell for hundreds of thousands of dollars, are bulky assemblies and often weigh many kilos, they are mostly used for oil exploration (detecting underground oil reserves through density contrast). But a low-cost and lightweight mass-produced alternative could be mounted on a drone instead of a low-flying aircraft, for simpler distributed land surveying and exploration through gravity mapping.

"To put things in perspective, 40μGalHz$^{-1/2}$ is sufficient in 1s to detect a tunnel with a cross-sectional area of 2m^2 and a length of 4m at a depth of 2m" the researcher wrote in his paper, so the gravimeter could be used to locate subterranean tunnels. Building contractors could find underground utilities.

"Unlike the electromagnetic spectrum, the gravity force can't be blocked" notes Middlemiss, "hence we can also detect the absence of mass, this is another way of imaging that could have defence applications, say to secure shipping ports.

Gravity mapping could become affordable not only to geologists monitoring volcanos (detecting the evolution of magma reservoirs prior to volcanic eruptions) but also to archaeologists seeking remnant building foundations. You could even conceive a fleet of drones flying synchronously to form a wide area density-contrast imaging array.

The researchers are aiming at further miniaturization and looking for industrial partners via QuantIC, the UK centre of excellence for research, development and innovation in quantum enhanced imaging. From the beginning, the design options and materials were chosen to favour easy industrialization using established processes. "A spin-off may be on the agenda", hinted Middlemiss.

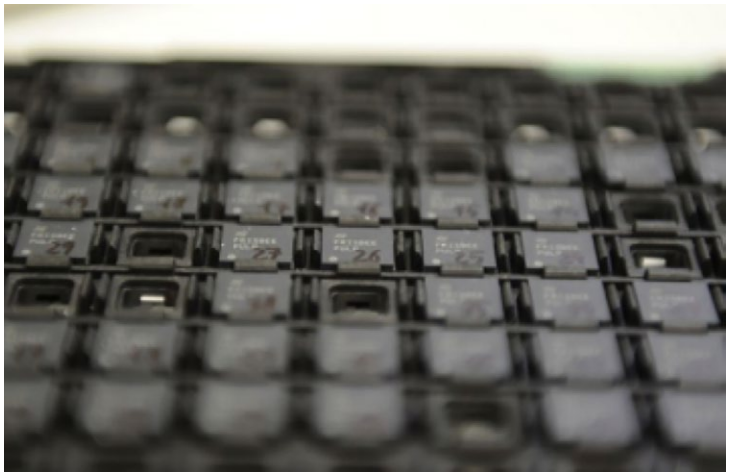
Swiss open-source processor core ready for IoT

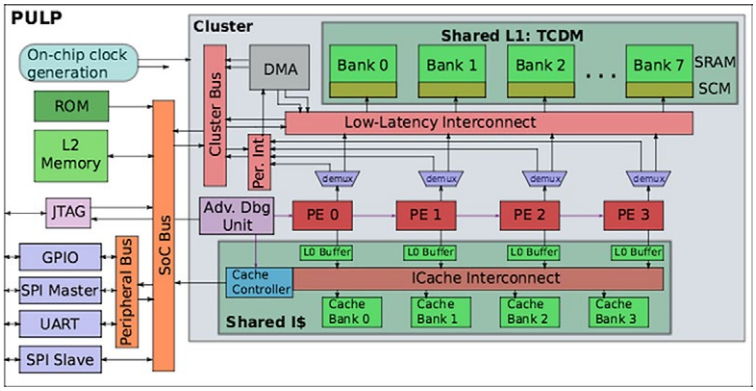
By Peter Clarke

Researchers at ETH Zurich (Swiss Federal Institute of Technology in Zurich) and the University of Bologna have developed PULPino, an open-source processor optimized for low power consumption and application in wearables and the Internet of Things (IoT).

Open-source and collaborative development is now standard practise in the software world – Linux being an example. While there have been hardware efforts, such as OpenRISC and Opencores, open-source hardware has gained the most traction at the board level. Examples include Arduino and Raspberry Pi, for which the PCB designs are publicly available. However, the chips on which those boards are based have remained proprietary.

Now a team led by ETH Professor Luca Benini, has put into the public domain the full design of one of their microprocessor systems, a derivative of the PULP (Parallel ultra-low power) project.





PULP designed with four processor cores. Source: ETH Zurich.

The 32-bit PULPino is designed for battery-powered devices with extremely low energy consumption. The arithmetic instructions are also open source: the scientists made the processor compatible with an open-source instruction set – RISC-V – developed at the University of California in Berkeley.

PULPino is a simplified version of the more general PULP, in that it has a single processing element rather than a cluster of four processing elements and has simplified instruction and data RAMs and was implemented in FPGA in 2015.

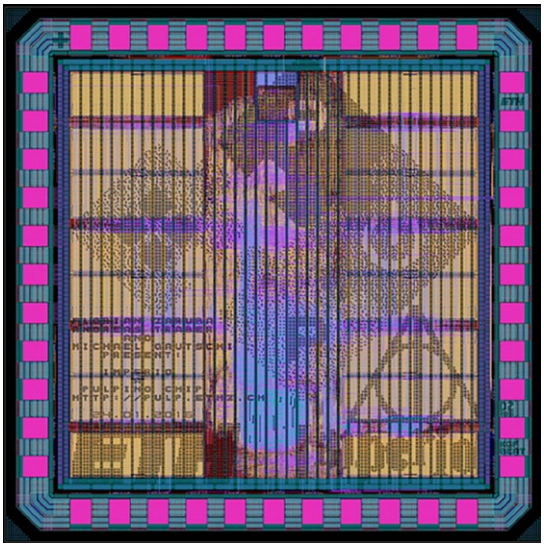
According to presentation materials (downloadable from www.pulp-platform.org) the PULPino core is called RI5CY and is a four-stage in-order pipeline implementation of RISC-V.

The core which is compared to a Cortex-M4 from ARM, has an instructions per cycle figure close to 1, support for the base integer instruction set (RV32I), compressed instructions (RV32C) and partial support for the multiplication instruction set extension (RV32M). It implements non-standard extensions for hardware loops, post-incrementing load and store instructions, ALU and MAC operations. To allow embedded operating systems such as FreeRTOS to run, a subset of the privileged specification is supported. When the core is idle, the platform can be put into a low power mode, where only a simple event unit is active and wakes up the core in case an event/interrupt arrives.

The PULP quad-core IC was subject of a tape-out in 28nm from Globalfoundries in November 2015 while the first PULPino implementation (called Imperio) taped out in January 2016 in 65nm CMOS from UMC. The PULPino platform is available for RTL simulation, for FPGA and SoC. It has full debug support on all targets and includes a port of FreeRTOS. Operating at a clock frequency of 400MHz and 1.2V the chip consumes 32.8mW.

The license to use PULPino will be "very liberal" and aligned with that of the lowRISC, another open-source processor in development, according to the presentation materials.

"In many recent examples of open-source hardware, usage is restricted by exclusive marketing rights and non-competition clauses," said Professor Benini.



Die of PULPino (Imperio). Source: ETH Zurich.

"Our system, however, doesn't have any strings attached when it comes to licensing."

The team reckon PULPino could be used to drive smartwatches, sensors for monitoring physiological functions or sensors for the Internet of Things. PULPino is being used in other research projects in Swiss and European research institutions and at Cambridge University.

Professor Benini said that PULPino should also be of interest to small and medium sized companies (SMEs) in Europe who often cannot afford to develop application-specific circuits. Development costs are reduced considerably with the open-source royalty-free design, which benefits SMEs as well as ETH, says Professor Benini.

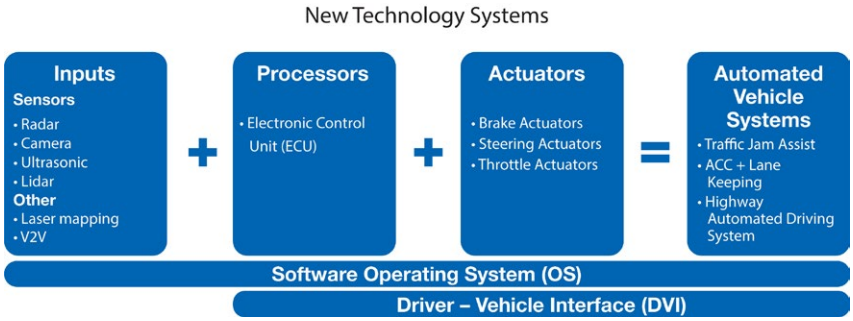
The coming revolution in vehicle technology and its implications

By Thomas Gage and Jonathan Morris

We are on the threshold of a radical change in vehicle technology, driven by crash avoidance technology and delivered by advanced driver assistance systems, or ADAS for short. As automobiles get smarter and increasingly connected, it is technologies like this that will mitigate the inherent risks as highways carry autonomous vehicles and potentially distracted motorists. Programmable devices like FPGAs and SoCs are at the heart of a software-led revolution.

Three vehicles, one revolution

Now, every day in California's South Bay, you can commonly see three vehicles representing three world-changing trends in the automotive industry: a sleek Tesla Model S rolling quietly past; a late-model sedan with an Uber "U" in the back window picking up a passenger; and a heavily modified Lexus SUV with a spinning LIDAR on the roof, driving itself down the street while a remote driver, anywhere in the world, collects data. These daily sights represent three technology-driven trends that are simultaneously arriving to significantly disrupt the automotive status quo: electrification, connectivity and autonomy. Each trend is moving at a different pace, but all three have one thing in common: software!



The basic ADAS architecture starts with a set of sensors that provide data on driving conditions to an ECU.

Software: refining today, revolutionizing tomorrow

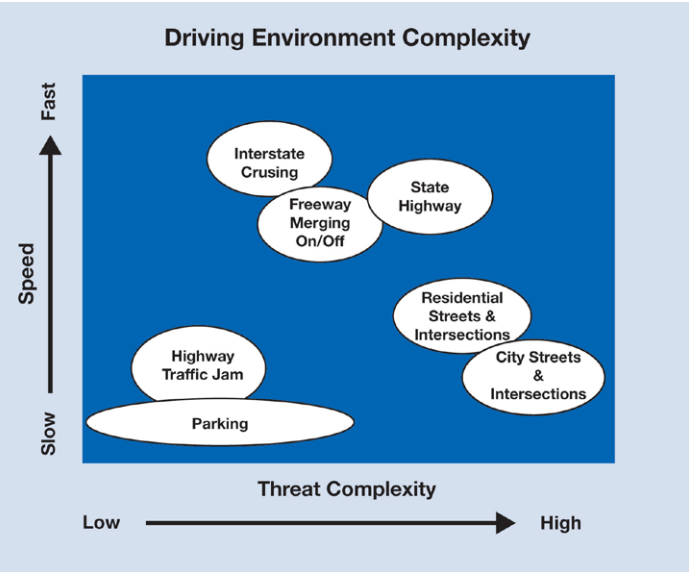
Since 2004, the costs of electronics in an average vehicle have doubled from 20 to 40 percent. Today's luxury vehicles commonly contain 100 microprocessors and run 100 million lines of software code, controlling everything from engine timing to infotainment systems.

We are now at a point where software, sensors and processors are delivering entirely new areas of vehicle functionality: not simply transitioning conventional functions from mechanical to electronic control. Both the ADAS systems of today and the autonomous driving systems of tomorrow will rely completely on software to make sense of data from sensors, cameras, the Internet, infrastructure and other vehicles.

Increased complexity of vehicles has already shifted the automotive value chain. The trends of electrification, connectivity and automation will only accelerate this shift in value toward those companies that create electronics and software, and away from OEMs that fail to innovate.

This shift will have two effects. First, software will become a critical market differentiator, pressuring OEMs to shorten product cycles and provide support and updates for legacy systems. Secondly, the shift to software allows new entrants to innovate in an industry with notoriously high barriers to entry.

In a typical ADAS-equipped vehicle, applications such as forward collision avoidance (FCA) are enabled by sensors providing data on the external driving environment to an electronic control unit (ECU).



ADAS software algorithms must account for road types, speed and threat complexity.

Thomas Gage is CEO and Managing Director at Marconi Pacific
www.marconipacific.com
Jonathan Morris is Senior Associate

This unit then uses software to determine whether a threat is present and operates brake actuators (or potentially, other countermeasures) to mitigate the threat.

The sensors available today for driver assistance applications are the hardware foundation for autonomous vehicles. Tomorrow's sensors will necessarily be smaller, faster and cheaper. But the real gap between the ADAS systems of today and the fully autonomous systems of tomorrow is seen in software. Regardless of how fast inputs can be processed, the software algorithms that will allow vehicles to drive themselves more efficiently and safely than human drivers in complex driving environments remain the biggest challenge.

Programmable devices accelerate innovation

Bridging the gap between dedicated hardware and innovative software, programmable devices such as Xilinx's Zynq-7000 All Programmable SoC are at the heart of today's most sophisticated ADAS systems and are quickly replacing much less versatile ASSPs. The combination of the Zynq SoC's ARM processors and FPGA logic on the same device has enabled OEMs to build highly sophisticated, all programmable ADAS platforms that can scale with automotive product lines and be upgraded with new enhancements to suit demanding and ever-evolving customer requirements.

Automotive OEMs can leverage the Zynq SoC in many platform configurations.

The device serves as a multi-sensor, multi-feature driver assist platform, a high-resolution video and graphics platform, a vehicle networking and connectivity platform, and an image-processing and recognition platform.

In these applications, customers implement algorithms for their design's most complex and compute-intensive functions in the logic portion of the SoC and implement serial processing functions in the on-board ARM processing system.

They leverage high-speed I/O to link to sensors and create highly reliable connections to automotive networks. Customers also leverage IP from SoC vendors, as well as their design tools and development environments, to quickly develop ADAS platforms.

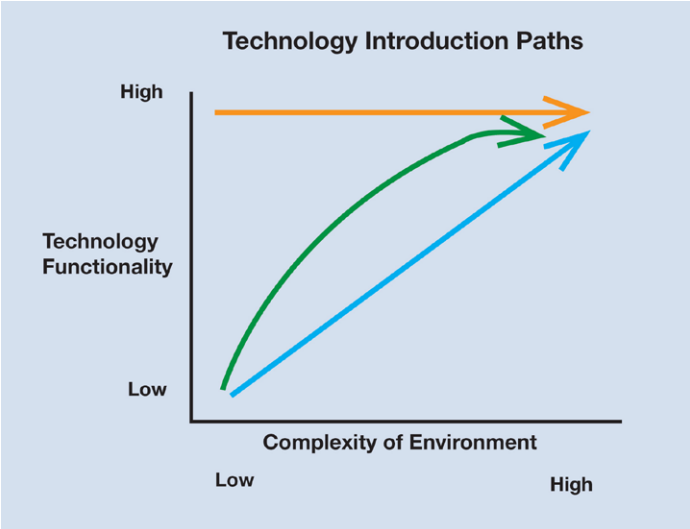
New introductions such as the Zynq UltraScale+ MPSoC version of the Zynq SoC will allow OEMs to create ever-more-sophisticated fusion systems with a programmable platform that can't be matched by any other silicon architecture.

Whilst OEMs are choosing different strategies to bring ADAS and vehicle autonomy to market, ADAS-equipped vehicles of increasing capability have already been introduced nearly every year since 2010 and continue to roll out annually.

Now that the early generations of this technology are available, how fast will consumers adopt it?

The relatively high cost of automobiles means that ADAS-equipped and autonomous vehicles are likely to be adopted at rates slightly slower than other modern technology, but they will still be adopted much quicker than conventional automobiles were.

As with the uptake of other new technologies, first movers and early adopters will drive early sales of ADAS-equipped vehicles, followed by gradual adoption by the majority of consu-



Simpler systems like "traffic jam assist" will roll out first, followed by systems able to operate the vehicle.

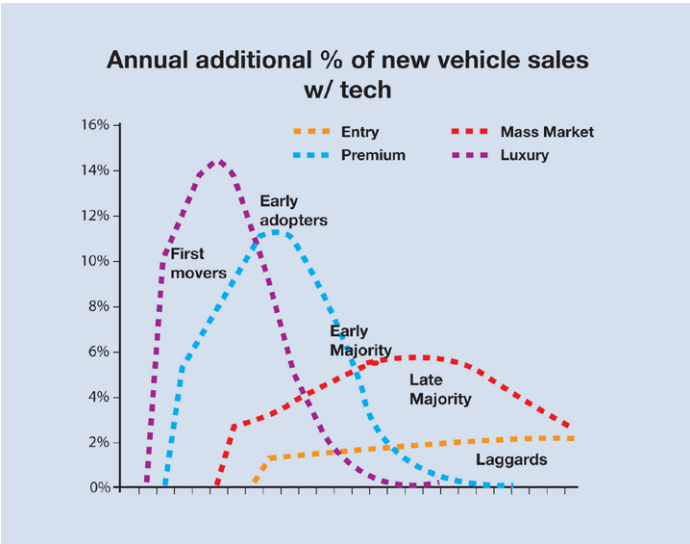
mers once the safety benefits have been proven and costs have fallen. This suggests that adoption will be driven by the benefits rather than throttled by costs.

Bearing out this conclusion, Marconi Pacific consumer research into ADAS and autonomy indicates that consumers will be initially drawn to the safety and convenience of this technology. Safety will be a large motivator for families as they learn how ADAS-equipped vehicles avoided crashes that might have injured or killed the vehicle's occupants.

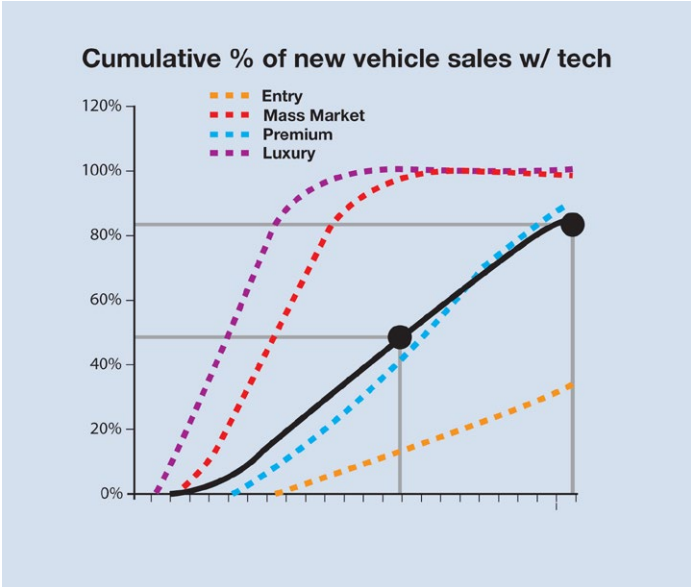
Another big driver will be time recapture. Being able to cruise along a freeway while paying limited attention to the road will be a significant accelerator of demand.

Marconi Pacific has built a diffusion model to better understand the pace of introduction of the technology and its uptake by consumers. The model is scenario based, with numerous inputs. Key factors include annual vehicle sales, ADAS technology introduction dates and fleet turnover forecasts.

The results are striking. In one run of the model, by 2035 more than 50 percent of vehicles and 85 percent of new-vehicle sales across all segments had one generation or another of



Additional sales for ADAS and autonomous vehicle (AV) technology will pick up as consumers see the safety and convenience benefits.



Cumulative sales for ADAS/AV technology could approach 85 percent of total car sales by 2035, according to one model.

ADAS-equipped or autonomous vehicles.

Of course, different levels of ADAS and of autonomy will have different impacts on society, including different levels of total annual crash reduction, different impacts on traffic congestion and different impacts on shared-vehicle, Uber-like services.

Auto ecosystem implications

The automotive sector and adjacent industries form a large ecosystem with pervasive reach across the global economy. As innovation in the form of electrification, connectivity and automation disrupts the status quo, the effects will be felt not just by OEMs, but also by numerous other sectors and businesses previously structured around conventional personal vehicles.

Companies that move quickly to take advantage of the opportunities are likely to succeed. Laggards will be the losers.

Ecosystem Implications of Driver-Assisted and Autonomous Vehicles

Industry Sector	Opportunity	Risk	Action Time Frame
• Vehicle OEMs	High	High	Now
• Traditional OEM suppliers	Medium	Medium	Now
• Tech OEM suppliers	High	Low	Now
• Motor Insurance Carriers	Low	High	Now
• Telecom Carriers	Medium	Low	Now
• Telecom platform providers	High	Medium	Now
• Security solutions	High	Low	Now
• Transportation agencies	Medium	High	Soon
• Auto – Repair/body shop/gas	Low	High	Later
• Auto dealerships	Medium	High	Now
• Big-data analytics	High	Low	Now

ADAS and autonomy will have a major impact on many ancillary industries besides just automotive.

Is car-to-car talk done deal in US?

By Junko Yoshida

Vehicle-to-Vehicle (V2V) and Vehicle-to-Infrastructure (V2I) technologies — collectively known as V2X — are leaving the test track and making their way onto public streets.

Sunnyvale, Calif. is the latest city serving as a real-world V2X testbed, for Nissan, Savari and UC Berkeley.

By gaining the support of the city of Sunnyvale, Nissan, which has a Research Center in Sunnyvale, has effectively shifted its V2X test program into the real world. The pilot project, spanning 4.63 square miles in Sunnyvale, includes three public intersections equipped with Savari's V2X-enabled road-side units.

In Sunnyvale, Savari and Nissan have deployed units at traffic lights to communicate with on-board units in cars. Data on traffic conditions at intersections is collected in real time, for broadcast to cars supporting V2X communication.

DSRC mandate?

Not everyone in the automotive industry is conceding V2X as a fait accompli, however.

It's been taking more than a decade for V2X to get commercially deployed. The Department of Transportation (DOT) has yet to mandate it, fostering a measure of skepticism in the automotive industry.

Roger Lanctot, associate director, global automotive practice at Strategy Analytics, for example, believes that cellular-based V2X deployment over LTE or 5G stand will have a better chance of success as a market-driven solution in the existing infrastructure. "[There is] no need to create an entirely new network—like what's required for V2X using Dedicated Short Distance Communications (DSRC)," he pointed out.

DSRC uses 75 MHz of spectrum in the 5.9 GHz band, which the Federal Communications Commission (FCC) set aside in 1999 for intelligent transportation systems (ITS).

Others believe that, although the DoT missed the 2015 deadline for a DSRC mandate, the government is moving ahead with it.

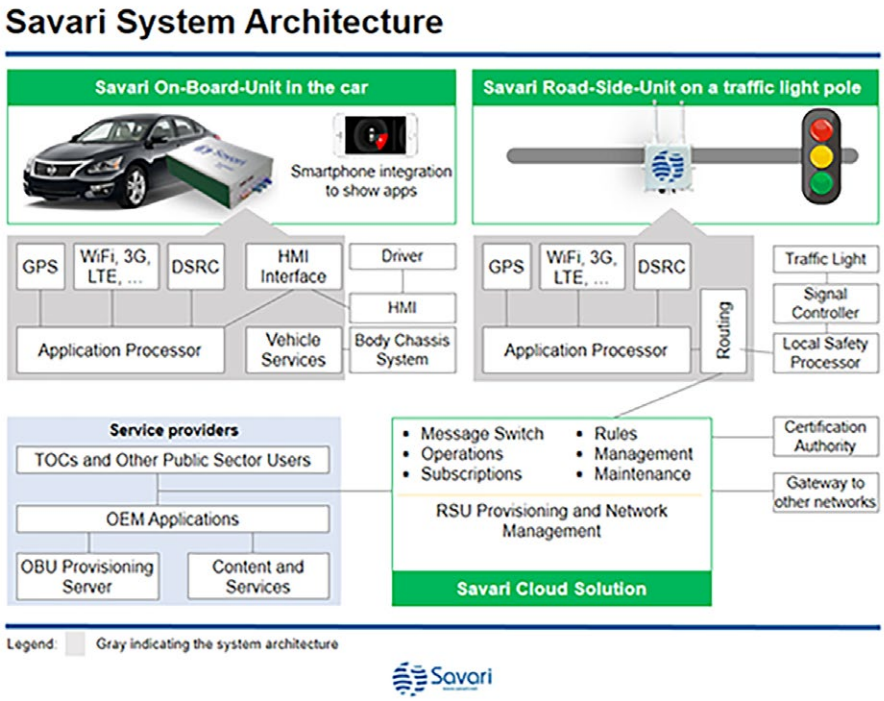
In an EE Times Radio show, Craig Aine, ADAS business development director at NXP Semiconductors predicted that the DOT will mandate DSRC by the second quarter this year. Scott McCormick, president of Connected Vehicle Trade Association also believes the mandate will come this year — but later — most likely in the fourth quarter.

Predictive safety

The number of tech companies joining the DSRC-based V2X ecosystem are on the rise. They believe V2X will eventually become a necessary companion tech element for autonomous cars.

Savari, an automotive tech startup, is a good example. The company is developing not just hardware (road-side units and on-board systems equipped with DSRC) but also its own software IPs and safety applications, which it says are available for licensing.

Paul Sakamoto, chief operating office at Savari, in an interview with EE Times, described V2X as "one of the few technologies that offer predictive safety."



(Source: Savari)

V2X-enabled vehicles and traffic lights will both know "kilometers ahead of time" what's coming down the pike, Sakamoto said. In turn, this will ensure intersection safety, ease traffic congestion and enhance fuel economy.

With the DSRC wireless technology enabling reliable communication between moving vehicles and fixed wireless infrastructure, cars will be able to alert drivers of upcoming congestion, construction, road conditions, or emergency vehicles. Cars could respond to a sudden slowdown by braking automatically.

Sunnyvale's Transportation Division hopes to apply data exchanged between vehicles and road-side units to enhance the operation of traffic light intersections.

Cars subject to fewer start-and-stop operations consume less fuel. V2X could lead to as much as a 15 percent savings in fuel consumption, according to the DoT.

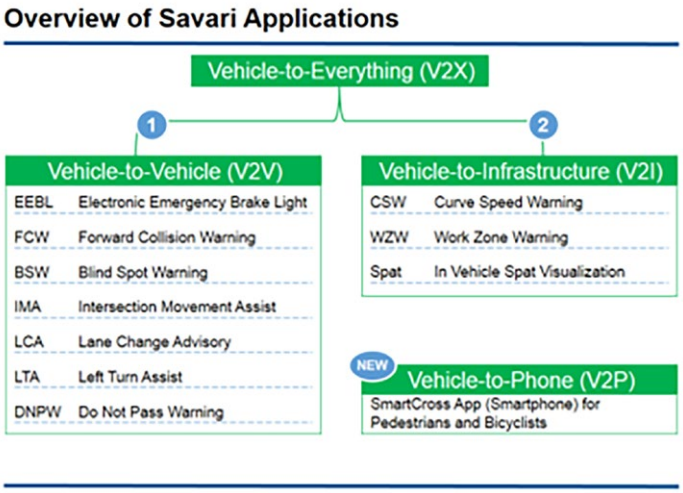
V2X and autonomous cars

But how will V2X help autonomous cars? Sakamoto acknowledged that automakers already have technologies like "lidars and image sensors" deployed in self-driving cars. However, "Neither can actually see beyond the visual range," he said. If a driver is not seeing it or paying attention to something, lidars

or image sensors aren't seeing it either, he said.

Although DSRC sometimes gets a bad rap as "more than a 10-year-old technology," Savari appears to have developed new IPs that might give it a fresh twist.

Savari's Sakamoto told EE Times, "We didn't invent DSRC radio, but we have developed a unique way of using DSRC data and processing it as a sensor. It results in actionable information."



(Source: Savari)

Savari, for example, claims that the company designed a DSRC-based technology that offers location data much more precise than GPS. "GPS offers location accuracy of several meters. We can currently reduce that to 1.5 meters," said Sakamoto.

Through a similar mechanism used by a Wide Area Augmentation System (WAAS), Sakamoto said that Savari can eventually attain centimetre accuracy in its location information.

Savari also understands individual cars' history (collected via V2X). When a thousand cars are stuck in congested area, Savari can filter the information down to the several most safety-critical cars in the jam, explained Sakamoto. "We've developed our own filtering algorithms."

Who's who in DSRC

Those in the V2X ecosystem that offer DSRC-based radio communication chips include NXP Semiconductors, Qualcomm, and Autotalks.

In 2014, Delphi Automotive revealed itself as the first Tier One to supply car-to-car communications modules to General Motors' 2017 Cadillac models. At that time, Delphi said that its V2V and V2I communication platform consisted of application software developed by Cohda Wireless and an NXP wireless chipset running DSRC based on an IEEE 802.11p.

Qualcomm's strong presence in the in-car cellular modem market is based on the DSRC technology in its WiFi chip, announced as part of its Snapdragon automotive solutions in 2014.

Nonetheless, it was the Cohda/NXP team, not Qualcomm, which snatched up the automotive industry's first big V2V and V2I commercial design win.

GM will be the first car maker to have a V2X system in a production vehicle, with their CTS Cadillac going into production at the end of 2016.

Israel-based startup Autotalks, partnered with STMicroelectronics, designs next-generation V2X chipset families. Its claim to fame is scalability and flexibility. Depending on car OEMs' plans to design V2X features – some want a complete standalone solution, while others prefer a V2X hardware add-on — Autotalks says it can meet all customer demands with flexible solutions.

Meanwhile, Savari (Santa Clara, Calif.) and Cohda Wireless (North Adelaide, Australia) are the two most notable vendors positioned to offer a comprehensive V2X package consisting of hardware (road-side units, on-board units), software and applications.

Savari's Sakamoto said that Savari sees its business not necessarily as a V2X hardware supplier. "We're willing to license our technology to anyone who wants to use some portion of our software running in their own hardware." It's entirely foreseeable for a certain part of Savari's V2X algorithms to run in different places in a car – like an ECU, a center stack or whichever platform an automaker decides to use, Sakamoto explained.

Similarly, Cohda's CEO said earlier this year in an interview with Telematic News, "As the market grows and matures, Cohda will move away from being a hardware supplier to become a software licensing company." He added, "This is evidenced by our recent announcements with both u-blox (who will license Cohda's V2X module) and Siemens (to whom Cohda will be supplying road side units)."

Savari's Sakamoto, acknowledging that Cohda is Savari's potential competitor, said that it's impossible for a single company to cover the whole gamut of V2X.

"We are increasingly seeing us working together" depending on projects.

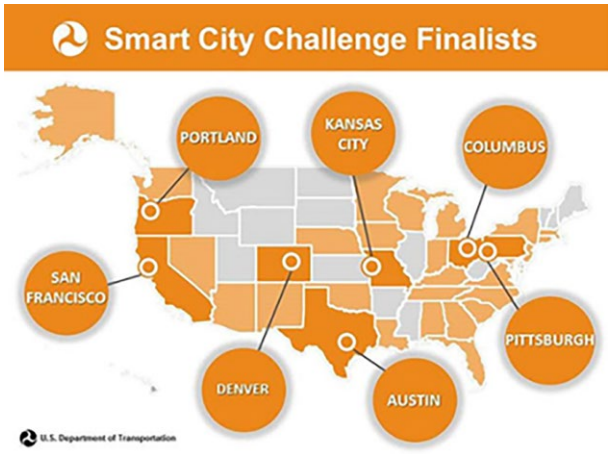
Savari offers advanced ITS applications in the form of plug-ins, which enable applications ranging from e-tolling, collision warning and pedestrian detection to traveller information alerts and transit signal priority. It covers not just V2V and V2I, but also V2P (Vehicle-to-Phone).

Operating systems to support the Savari SDK include Linux OS and now automotive-grade QNX.

Smart city challenge

To improve transportation infrastructure in communities isn't just a pipe dream. Given the fact that more than 78 medium-sized U.S. cities applied for the DOT's Smart City Challenge (issued in December, 2015), the idea appears to be catching on.

The DOT has pledged up to $40 million to one city to help it define what it means to be a "Smart City "and become the country's first city to fully integrate innovative technologies – self-driving cars, connected vehicles, and smart sensors – into its transportation network.



(Source:US DOT)

The winning city will be announced in June from seven finalists that include Austin, Texas, Columbus, Ohio, Denver, Kansas City, Pittsburgh, Portland, Oregon and San Francisco.

Savari's Sakamoto said, "We're planning to pitch our technology to every single one of those seven cities."

Opportunities and challenges of over-the-air software updates in automotive

By Stephane Strahm

The Internet of Things (IoT) and the increasing value and capabilities of software deployed within and outside the car are changing the automotive industry. A major enabler for this new software-powered paradigm will be the ability to update software 'over-the-air'. Stéphane Strahm, Director Automotive Products Engineering, Wind River, looks at the opportunities and the challenges for carmakers.

The growth of software in cars for both in-vehicle infotainment (IVI) and under-the-hood applications, such as ADAS (advanced driver assistance systems) and autonomous driving, is posing challenges for the automotive industry. For example, how best to deliver new applications and new software releases to vehicles that are already on the road?

The value proposition in automotive has changed significantly compared to some four decades ago, where approximately 90% of a vehicle's value was tied to solid and tangible aspects of the Bill-of-Material. In the coming decade, that value is expected to be drastically reduced with 50% or more of the vehicle's value being defined by software and a better user experience, where new applications can create value many times greater than that of the actual assets – see figure 1.

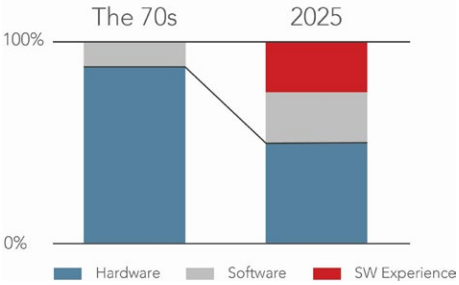


Fig. 1: The changing value of automotive from hardware to software and new applications

Another key trend that is driving the development of the next generation of vehicles is the emergence of the Internet of Things (IoT). Through the use of software, automotive systems are becoming more connected within the car but also with the outside world. Software is helping to create differentiated driving experiences. The growing role of software in the car and the increasingly interconnectivity of its systems brings a number of challenges, which means that car OEMs will need to have a strong grasp of the holistic software environment to orchestrate a successful vision of the connected car.

Development and deployment lifecycle

The updating of software/firmware over-the-air (SOTA/FOTA) is being seen as a critical methodology to manage software updates with the latest revisions for the entire lifecycle of a system – from the initial architecture design of the hardware and software to the life of the car on the road which could be 10 years or more. It is still very early days for OTA and actual deployment is still in the nascent phase. However, the potential benefits are many, both before and after a car rolls off the production line.

During the vehicle development cycle, software updates will have to be managed across a fleet of pre-production vehicles and usually software is the last thing to be updated prior to the release of a car. The car of today is likely to have a hundred or more control systems or ECUs (electronic control units) and development teams will be faced with several software revision cycles, which could be a versioning nightmare.

In addition, car development at major OEMs does not happen in a single geographic location, but is spread across several development centers.

Therefore the management and monitoring of software during development is a challenging prospect.

However, delivering software updates wirelessly, or over-the-air, delivers the potential to significantly ease the development process and avoid time-consuming individual car updates, which is a massive cost and time advantage.

In addition, the ability to use OTA to update software or fix issues when the car has left the factory brings significant advantages. It is more convenient, efficient and lower cost than physically bringing cars into dealers or garages. A robust and dependable OTA strategy means that OEMs can update the systems in near real time over the lifetime of the vehicle. Additionally, as the useful life of vehicles continues to grow, there is further opportunity to increase the value of the deployed vehicle base with continuous improvement of the experience, which can also open new revenue streams.

Applications

For IVI applications, consider the use case of navigation with OTA. Maps on our mobile devices are updated continuously, whereas map updates for a car's navigation system may require a customer to visit a dealership every year or so, which tends to lead to low adoption as well as low customer satisfaction. In addition, cars typically will initially come with a subset of maps such as those for the home country or possibly the continent. OTA capabilities can enable maps to be downloaded automatically, and as required, thereby reducing the memory footprint

Consider now the huge opportunity for OTA updates on under-the-hood vehicle systems.

Stephane Strahm is Director Automotive Product Engineering at Wind River - www.windriver.com

Many vehicle functions that were once mechanically operated, such as steering, acceleration and braking, are electronically actuated today. As these functions are critical to vehicle operation, it is essential that they operate with the latest software or necessary updates, as this may have a real impact on safety.

For example, an important use case is software-related recalls or updating software due to a bug. The costs of managing warranty and recalls can have an impact on millions of vehicles and across many geographic markets, potentially costing many billions of dollars for an OEM. The cost per vehicle can be in the hundreds of dollars per vehicle by conventional means, not taking into account the time required to perform the update. However, OTA can dramatically reduce the cost and time of software update implementation, benefitting both the carmaker and their customers.

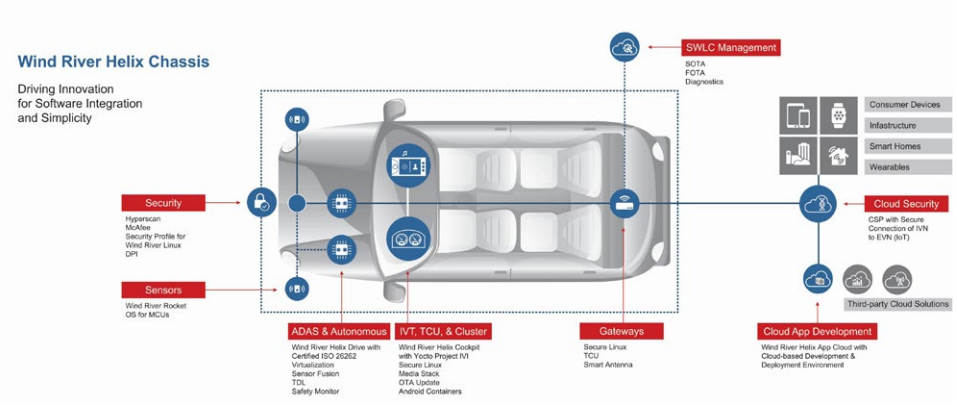


Fig. 2: Wind River's Helix Chassis automotive development suite including FOTA/ SOTA management via Helix Cockpit.

Connectivity

Although OTA makes it possible to upgrade multiple systems in the car, implementing an OTA system introduces new challenges for carmakers such as security, robust connectivity, bandwidth, and also designing for the infrastructure in different global markets. Specific questions on OTA include software update verification; potential impact on other systems within the car; and unauthorized access to vehicle software. In addition, the potential use of OTA may challenge existing elements of the current automotive industry: for example, potentially reducing customer visits to dealerships can have a significant impact on the dealership revenue model.

To enable real-time data usage, connectivity is a key piece of the OTA puzzle. As updates will need to be properly implemented, today carmakers are performing OTA for select systems such as IVI applications, rather than those under-the-hood. In addition, these OTA updates are being performed in well-controlled environments such as in dealerships where updates can be properly supervised and verified. But over time, connectivity speeds and bandwidth will improve with greater investment in data networks and communications infrastructure in general. Data centers will grow and many of them will be specifically dedicated to specific automotive profiles. In addition, the increasing realization of the IoT – gathering and using real-time and actionable insights from the car and its surrounding environment – will continue to create new value propositions for automotive.

Security

Security is clearly a priority for OTA: as well as the loss of private information, a software hack could compromise non-IVI systems and pose significant safety risks. Securing the car is fundamental challenge for the automotive industry that will be need to be addressed in terms of hardware, software and the cloud, and especially the applications that move between all these.

There are many places along the data connection chain that need to be secured and to follow the appropriate protocol: this begins with the embedded device and goes up to the data center, potentially being hosted by the OEM. Partitioning is a particularly important technology to mitigate risk. At a basic level this means separating critical functions so that accessing one function offers little to no risk to an adjacent function, but it offers significantly more than this. Wind River has a substantial knowledge base in understanding how to partition, transmit/ receive and validate data.

An absolute must for security is the development of standards and this will need to involve government agencies, car companies and technology/software vendors. Transit authorities such as the NHTSA are currently in the process of defining standards for safety and security. However, this effort transcends more than just OTA and has an impact on connected vehicles and related issues such as autonomous driving.

Helix Chassis

To help carmakers meet the challenges of OTA and other next-generation automotive technology challenges, Wind River has introduced the Helix Chassis framework of products (figure 2), which includes offerings such as Helix Cockpit and Helix Drive and provides continued expertise for infotainment, telematics and digital cluster systems; safety-oriented systems including ADAS and autonomous driving; and cloud-based development tools and enhancements for the applications.

Helix Cockpit was designed to meet the intersecting needs of automotive and the IoT and is a GENIVI-aligned and Linux Yocto Project based software platform that helps customers develop IVI, telematics, and instrument cluster systems. It is a flexible, extensible and pre-integrated platform that supports various industry-standard hardware and HMI tools. It can welcome market leaders SOTA solutions such Arynga, Movimento or Redbend. Cockpit also provides access to Wind River Helix App Cloud – a cloud-based software development environment for building IoT applications across multiple development centers.

Additionally, Helix Drive is a software platform based on Wind River RTOS (VxWorks) that helps carmakers develop ISO26262-certifiable safety-critical applications.

The next generation of vehicles will increasingly make use of the software utilities that we already have in our personal connected devices, and OTA is an important enabler to deliver a richer and more user-defined driving experience via automotive-specific applications and better real-time access to information. Carmakers are already beginning to tap into the vast potential of OTA, today primarily focusing upon IVI functionality.

As many of these new IVI technologies are more costly to implement, these are likely to be integrated into higher-end or luxury vehicles before trickling down to higher-volume cars. However, as OTA processes become more solidified and proven, OEMs will migrate to OTA for the implementation of software updates for the more critical under-the-hood vehicle functionality over time, and increasingly across a more diverse range of mass-market cars.

Ficosa & Panasonic partnership yields smart rear-view mirror

Automotive safety solution provider Ficosa (Barcelona, Spain) has co-developed an intelligent rearview mirror (IRMS) with display manufacturer Panasonic (Osaka, Japan).

The system features an integrated Panasonic LCD screen in the structure of what looks like a traditional rear-view mirror. It works as a mirror or as a monitor that relays images from the cameras located at the rear of the vehicle or even from within the vehicle.

The camera built into this intelligent mirror is digital and offers a high resolution image. Ficosa offers car OEMs to integrate the camera in various locations of the car according to their preferences, either inside or outside the vehicle.

The interior mirror enhances the driving experience and increases safety and driving comfort. This solution extends the rearward field of vision up to a value of 50° (more than double compared to a traditional mirror, says Ficosa), which considerably reduces blind spots. It also attenuates the glare and improves visibility in low light areas.

The IRMS also stands out for its ability to work split screen as a mirror and monitor simultaneously. In this operating mode it can also project the image of other devices integrated in the vehicle as parking camera or even internal cameras to control children, among other devices. Additionally, it will also allow the inclusion of ADAS (Advanced Driver Assistance Systems) in this vision system, giving information about surrounding vehicles to the driver.

Currently, Ficosa is already working with different car manufacturers on the integration of intelligent interior rearview mirror, customizing it according to their requirements. It is expected that the regulation in this field will be approved in a European level by the middle of this year and it is foreseen that vehicles can circulate with this system integrated by the beginning of 2018.

Last June, the Japanese multinational acquired 49% of Ficosa shares and both companies have partnered to increase their technological capacity and integrate complementary technologies to lead the transition of the automotive market in new product categories.

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Semi-autonomous trucks flock together in platoons

By Christoph Hammerschmidt

Fleet operators have tracked position and status of vehicles and their valuable loads more or less since the inception of satellite navigation and mobile networks. Now Daimler Trucks goes one step further, by demonstrating how multiple trucks can be connected together via V2X (vehicle-to-everything) communications technology, led by a semi-autonomous guidance vehicle. Such "platoons" help truck operators save on fuel by up to 11%, depending on a vehicle's position within the platoon.

The pivotal achievement in this context is an electronic control unit called Highway Pilot Connected. This is an evolved version of Daimler's Highway Pilot, introduced two years ago.

All trucks that are connected in such a platoon are equipped with the Highway Pilot Connected. Providing linear and lateral guidance through active steering mechanisms, this unit enables each vehicle in the platoon to drive independently as autonomously driving trucks. In contrast to its predecessor, the Highway Pilot Connected however enables the vehicles to communicate with each other and with the infrastructure by means of the V2X technology, an implementation of the IEEE 802.11p radio standard. Safety-critical messages can be passed along within 0.1 seconds.

An important feature of the Highway Pilot Connected is the high-resolution digital road map. Thus, the trucks are always aware of the road topology, knowing when a bend or downslope requires the vehicles to slow down.

The driver, monitoring the system, receives information about the status of the platoon and the traffic situation via an 8-inch monitor in the instrument panel. This displays route information as well as the vehicle's own position within the platoon. Each driver therefore knows the current number of platoon members and his position within the group.

In addition the individual drivers are always kept aware of the traffic situation. A camera in the lead vehicle keeps the situation ahead of the truck under surveillance. Its images are transferred to all the vehicles in the convoy by WLAN, and shown on each monitor.

On motorways the semitrailer combinations form a platoon with a distance of only 15 meters apart. This small distance considerably reduces air resistance, thereby lowering fuel consumption and CO_2 emissions by around five percent. On level roads this makes fuel consumption figures of around 25 l/100 km possible for a loaded semitrailer combination with a gross weight of 40 t.

This corresponds to a consumption of only 0.66 l/100 km per tonne, or CO_2 emissions of 13.3 g per kilometre per tonne – well below that of any passenger car with an internal combustion engine.

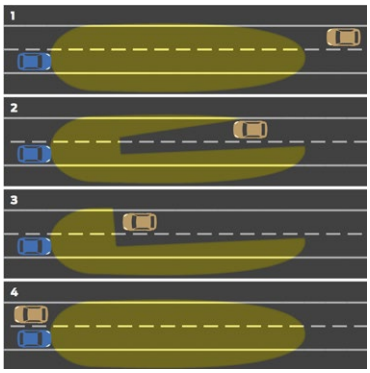
Measuring drives on a level test route with three semitrailer combinations at a constant speed of 80 km/h have even shown a fuel economy advantage averaging seven percent. This advantage is at different levels depending on the position in the platoon: In a three-vehicle platoon the lead vehicle has a fuel advantage of two percent, the middle vehicle eleven percent and the rear vehicle nine percent. These differences are due to the differing aerodynamic effects on the individual vehicles.

The Highway Pilot Connect is currently approved for platoon driving within the German state of Baden-Württemberg, for most of the A81 autobahn from Lake Constance to Würzburg greater Stuttgart area. Daimler has received an additional approval for the A52 in the greater Düsseldorf area, where Daimler demonstrated the technology to the press.

Dazzle-free high beam under camera control

By Christoph Hammerschmidt

Ford Motor Company has developed a technology that helps to improve the safety of oncoming driver in the night: A camera, located behind the windscreen, identifies oncoming traffic and automatically switches the headlight to low beam. It also recognises rear lights of cars and bikes – at distances up to 800 metres (half a mile).



Studies have shown that the high beam in automated headlights are used up to ten times more frequently than headlights with manual control. Since high beam is unnecessary if it is not used, Ford has developed a new headlight technology that enables drivers to utilise the high beam on dark roads without the need to switch to low beam manually. A windscreen-mounted camera identifies the headlights of oncoming vehicles as well as the rear lights of cars and bikes and moves a cover to the headlight's projecting lens that shades the respective sector in the cone of light. The result: No more dazzling.

The dazzle-free high beam is available for the new Ford models S-Max, Galaxy and Edge as a feature of the carmaker's adaptive LED headlights whose light beams automatically adapt brightness and beam angle to the vehicle's situation. The beam automatically follows curves and intersections and thus improves sight and safety during night rides. In addition to moving a cover to certain beam segments, the headlights also modify their light field according to the speed and thus ensure optimal illumination in all driving situations, Ford advertises.

PSoC Eval kit speeds CAN and LIN component design

Cypress Semiconductor's CY8CKIT-026 CAN and LIN Shield Kit features two CAN transceivers for high-accuracy, high-speed transmissions, two LIN transceivers and Arduino compatible headers. Additionally, the kit includes five example projects that demonstrate the CAN and LIN capabilities of PSoC 4. The CY8CKIT-026 CAN and LIN Shield Kit enables designers to quickly create their own projects with easy-to-use CAN and LIN slave components in Cypress's PSoC Creator Integrated Design Environment (IDE) or by altering code examples provided with this kit. The IDE simplifies system design and accelerates time-to-market by enabling concurrent hardware and firmware design. PSoC Creator works with PSoC Components—free embedded ICs represented by an icon in the IDE—to enable rapid prototyping of end applications while minimizing PCB redesigns and firmware changes.

Cypress Semiconductor
www.cypress.com

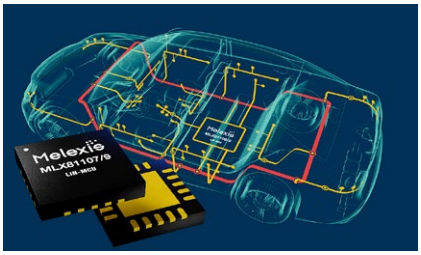
Honda, Hitachi develop breathalyzer smart car key

Hitachi Ltd. and Honda R&D Co. Ltd. have developed a prototype of a portable alcohol detector that can distinguish human breath from alternative gases and be integrated into a smart automobile key. This is the basis of a smart key for automobiles that cannot be driven until somebody's breath has been tested for alcohol. If that test is failed then the car can be locked not to start. The sensor is an oxide insulator sandwiched between the electrodes. The water vapor from the breath is adsorbed on the insulator and then an electric current flows between the electrodes. The ethanol concentration is measured by three sensors tuned to detect ethanol, metabolized acetaldehyde in breath after drinking, and hydrogen, respectively. This method improves accuracy by about a factor of three compared with those that use only an ethanol sensor for measurement. Also, the device is capable of measuring an ethanol concentration of 0.015 mg/L compared to 0.15 mg/L of the alcohol which constitutes being "under the influence of alcohol" and a charge of drunk driving in Japan.

Honda R&D Co. Ltd.
www.honda.com

Cost-optimised LIN controllers enable new applications

With the MLX81107/MLX81109 LIN transceivers, Melexis is addressing the demand within the automobile industry for sophisticated LIN-based switches, actuators, drivers, sensor interfaces and LED lighting systems. The MLX81107 and MLX81109 both incorporate a physical layer LIN transceiver, LIN controller, voltage regulator, 16-bit RISC-based microcontroller, 32kBytes of Flash memory and 20-channel analog-to-digital converter (ADC), as well as possessing 16-bit pulse width modulation (PWM) capabilities. The LIN protocol handler is compliant with LIN 2.0, LIN 2.1 and LIN 2.2, as well as SAE J2602. The ICs have 4 high voltage capable (12V direct) IOs, plus 8 low voltage capable (5V) IOs. Through these interfaces, communication with the vehicle's LIN infrastructure is facilitated. Every IO can be programmed to control the application components using the built-in Flash memory resource.



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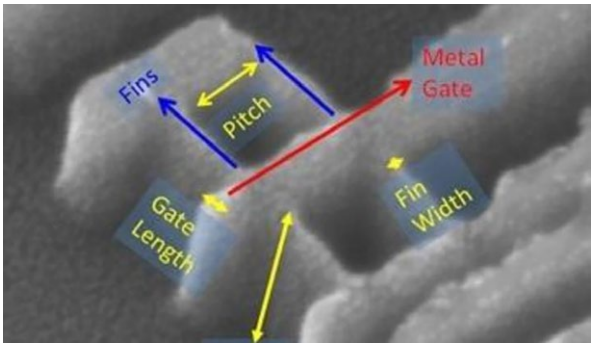
Synopsys touts 'visually assisted automation' for FinFET design

By Dylan McGrath



EDA and IP vendor Synopsys Inc. introduced a new custom design tool that aims to help offset design challenges posed by the era of FinFETs with an intuitive concept dubbed visually assisted automation.

The incorporation of FinFETs—3D transistors—create significant challenges for designers, including increased design rule complexity, additional layers of interconnect and the need for the use of double-pattern lithography to produce them. Synopsys estimates that it takes about three times more effort to do a custom designed circuit with FinFETs than it would take to do an equivalent planar circuit, according to Dave Reed, director of marketing for Synopsys' analog/mixed-signal design tool group.

"FinFET brings a significant challenge to custom design," Reed said in an interview with EE Times.

Synopsys claims that the new tool, Custom Compiler, can reduce many tasks associated with custom design from days to a matter of hours. The tool is also said to reduce iterations of designs and help enable reuse.

According to Reed, Synopsys first became fully aware of the challenges posed by custom designs with FinFETs from the company's team of intellectual property developers.

"The nice thing about these folks is that because they are doing IP development, they are among the very earliest users of new nodes," Reed said. "We have been doing a lot together, learning how to improve custom layout for FinFET designs."

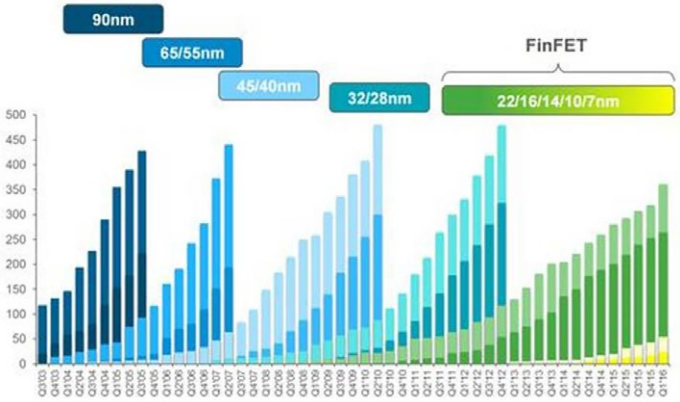
Custom Compiler bucks the trend in custom analog design tools of moving toward constraint-driven design methodologies. Rather than require designers to write code or constraints, Custom Compiler uses what Reed calls a visually-based, successive refinement approach.

"Visually assisted automation uses the natural language of a layout person, which is graphic manipulation," Reed said.

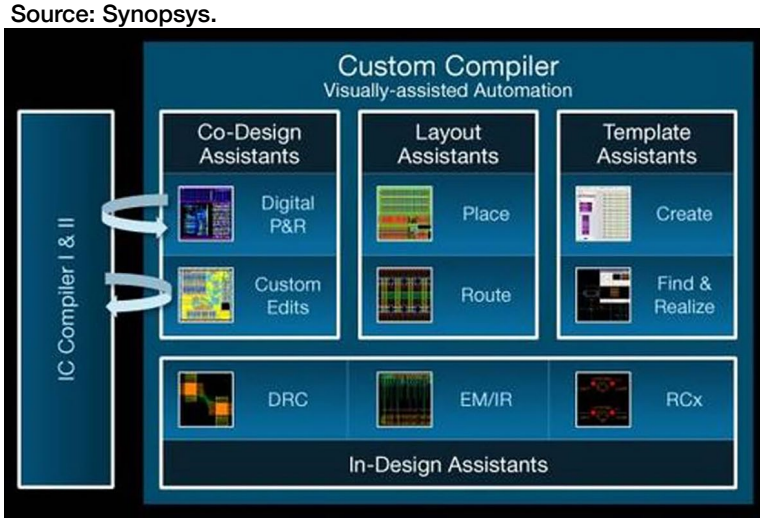
"We don't make them write constraints, we don't make them write code, and we don't try to automate something by writing a complex array generator. Instead, we do our best to infer constraints from the work that the layout person is doing."

Synopsys believes that constraint-based design has some real flaws that have prevented it from taking off, Reed said. While the idea behind the methodology makes sense for digital designs, he added.

"But in analog, we have a very complex set of constraints to describe what we really want to happen," he said. "A lot of what happens is human intuition. Some of the things that we have to tell the tool are very complicated. What people have found is that by the time they got done editing the text constraints, they may as well have just done the layout themselves."



Synopsys says the growing number of FinFET design starts and tapeouts point to the need for a new custom design solution. Source: Synopsys.



Block diagram overview of Custom Compiler, including integration with IC Compiler. Source: Synopsys.

The other problem with constraint based design is what Reed refers to as the "take it or leave it approach," he said. Constraints are input into the tool and it spits out a design. And if the designer doesn't like the solution, the only recourse is to go back in and edit the constraints, then push the button again. "People find that that's not a real converging solution," Reed said.

Reed stresses that Custom Compiler provides all the basic functionality that users are looking for. At its root, the tool is a layout editor and a schematic editor that provides "all the polygon-pushing and schematic features" that layout designers are accustomed to, he said. But on top of that, Custom Compiler provides visually assisted automation capabilities and "assistants" in four categories:

Layout assistants to

provide visually guided automation of placement and routing; In-design assistants to reduce design iterations by catching physical and electrical errors before signoff; Template assistant to enable reuse by making it easy to apply previous layout decisions to new designs; and co-design assistants that combine Synopsys' IC Compiler and Custom Compiler into a unified solution.

Reed said that while users do not need to deal with writing constraints, by using Custom Compiler they are actually creating constraints "under the covers" in a way that is transparent to them by noting how the user arrives at a solution and offering that same solution for reuse elsewhere in the design and in future designs.

"In analog design, everything is variations on a theme," Reed said.

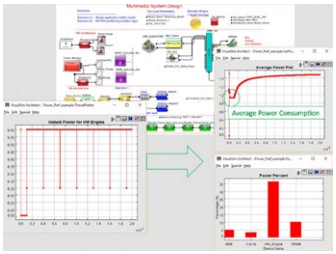
"There are the same basic circuit types being used over and over and over again. We thought if there were a way for us to abstract that pattern of what the layout person had done and save it so they can reapply I later, that that would be a real time-saver."

Reed said Synopsys has been using Custom Compiler internally since last summer. Several customers have been using the tool since late last year, he added.

In support of the product's release Wednesday, Synopsys announced that users include STMicroelectronics NV, GSI Technology Inc. and Asahi Kasei Microdevices Inc. Synopsys also announced that Custom Compiler has been certified for Taiwan Semiconductor Manufacturing Co. Ltd.'s 10nm and 7nm process nodes.

Cycle-accurate power analyzer targets system-level models

Mirabilis Design's VisualSim Power Analyzer is the first use-case driven power analysis software for both systems and semiconductors, according to the EDA tool vendor. The power equations and state-machine are fully integrated into all



the major library blocks in the VisualSim Architect hardware library. The system model can be used to experiment with power management schemes, scheduling algorithms, buffering, power gating, system-level decisions (burst length to memory, redundant systems and topology) and arbitration. Current generation power analyses are restricted to spreadsheets with use-cases as the columns and the rows as the devices, or power modeling at RTL/Gate Level. The former provides average power consumption values and the latter helps to make implementation decisions and not architectural decisions. VisualSim creates a major step in system design by migrating from analytical to dynamic power computation, add more power metrics, gain visual insight and create better quality products. The Power Analyzer library enables designers to add power attributes via a spreadsheet in an existing system-level model in VisualSim.

Mirabilis Design
http://mirabilisdesign.com

Interoperable PDK opens up analog design

Sensor and analog IC vendor AMS AG (Premstaetten, Austria) has made available a "interoperable" process design kit (iPDK) for its 0.35-micron analog speciality processes. Such iPDKs are based on the OpenAccess database and use stan-

dard languages as well as a unified architecture to enable interoperability among multiple EDA vendor tools. The iPDK v4.10 includes parameterized device layouts (PyCells) scripted using the Python programming language and support the C35 (CMOS), S35 (SiGe-BiCMOS), and H35 (High-Voltage CMOS) manufacturing processes. The iPDK has been tested & qualified with Keysight EEsof EDA Advanced Design System (ADS) 2016.01 and Synopsys Galaxy Custom Designer 2014.12.

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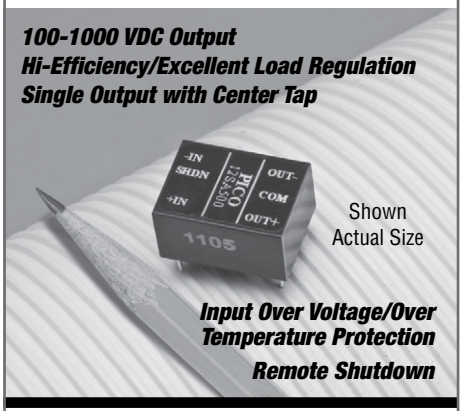

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Understanding your chip's age

By Oliver King

In this Q&A about in-chip monitoring, Moortec's CTO, Oliver King shares his insights on the relevance of understanding the mechanisms for chip ageing and how one can take this ageing into consideration for product design.

Q: Why is understanding your chip's age important?
A: Semiconductor devices age over time, we all know that but what is often not well understood are the mechanisms for ageing or the limits that will cause a chip to fail. In addition, there is bound to be a requirement for a minimum lifetime of a device which will depend on application but could be two or three years for a consumer device and up to twenty-five years for a telecommunications device. Given that lifetime requirement and often poorly understood ageing processes, many chips designed today are over designed to ensure reliable operation. If you understand that ageing process or better still can monitor the ageing process then you can reduce the over design and potentially even build chips that react and adjust for the ageing effect, or predict when that chip is going to fail.

Chips at the moment are not getting anywhere near their total lifespan because in most cases there isn't any in-chip monitoring taking place. I sometimes use the analogy of a rental car which you want to give back with an empty fuel tank. If your chip has a defined lifetime, then you want to run it as hard as you can to just perform within spec for the lifetime, or looking at it the other way, you want to hand your rental car back just as you run out of fuel.

Q: What are the effects and mechanisms of ageing?
A: There are a number of mechanisms which contribute, the most notable ones are electro-migration, hot carrier effects, and bias temperature instability. Whilst some of this can be mitigated through design techniques, and CAD tools exist to help with that, they can only go so far. In the case of bias temperature instability, the mechanisms are not fully known. Whilst traditionally only negative bias temperature instability (NBTI) was considered an issue, now, with the introduction of high K metal gates at 28nm positive bias temperature instability (PBTI) is now a problem as well.

The result of BTI is to raise threshold voltages, and the effect is very temperature dependant, so without a good model of device use it is hard to predict and thus design for. In addition, ageing effects in general are, by nature, hard to measure because it takes a long time even with acceleration techniques such as HTOL to get a device to end of life.

Q: How can we help predict device lifetime?
A: From Moortec's perspective we are working on monitors that can be used to measure the ageing process of a device in the field, by having reference structures and comparing them to live structures, we can compare the two over time. This is one application that is being used at the moment, alongside using the information to adjust the supply to bring the chip back to the performance level that you expect, or need. This is actually quite common, particularly in devices where there is a requirement for a particular throughput.

Q: How does this help with choosing the lifestyle or your chip?
A: The thing is that ageing is complex and very dependent on use case and environment. In most modern applications neither of those is well known and often will vary over time itself.
If we take the smartphone as an example, there will be modes where it is doing very little - where the clock frequency is low, the voltage supply is low. At the other extreme it will be playing HD video - the clock will be run at high rates and the supply will be correspondingly high. Obviously if you took that device and left it in the low power state it would age at a significantly lower rate than if you left it in the high power state. The trouble is at design time you don't know what that ratio is. Of course this example is actually already a simplified case because more often than not there will be more than two states so you have to make assumptions about time spent in each state, and build margins in to cope with the unknowns. By allowing the system to monitor that ageing then potentially you can optimise DVFS schemes, you can predict lifetime or perhaps even reign in certain modes to insure that a particular lifetime is met.

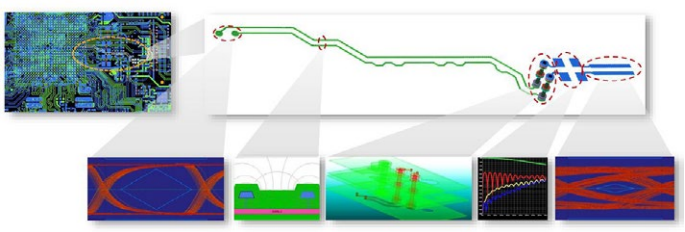
Another example is the bitcoin mining application. This is at the other end of the scale, where devices are manufactured to sit in large arrays. Each chip will vary with process and they will age differently partly as a result of process variation, and partly because their loads won't always be equal. If you can monitor all those conditions, then you can optimise each of those chips to run at peak performance.

Oliver King is the Chief Technology Officer of Moortec Semiconductor - www.moortec.com

Packing signal and power integrity, 3D-electromagnetic solving, and rule checking in one tool

In its latest HyperLynx release, Mentor Graphics integrates signal and power integrity analysis, 3D-electromagnetic solving, and fast rule checking into a single unified environment.

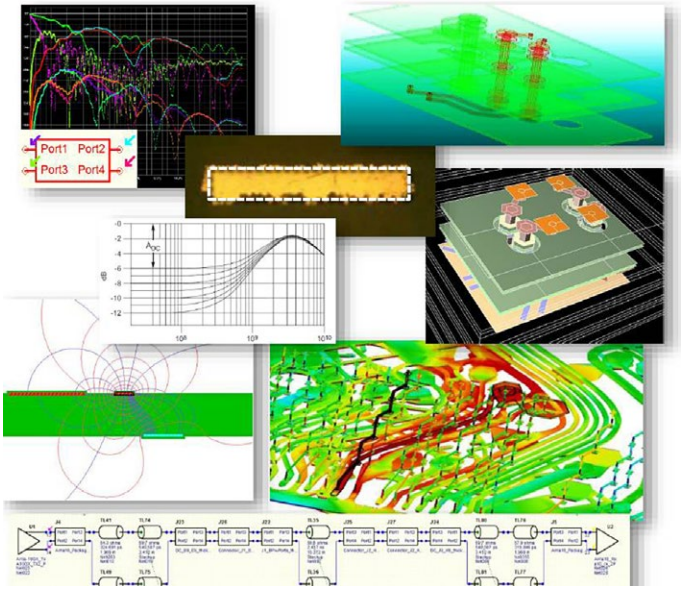
Aiming at high-speed digital PCBs, the company puts forward a tool that offers designers a complete set of analysis technology, spanning a wide range of underlying simulation engines and a graphical user interface (GUI) that supports both



quick/interactive and exhaustive batch-mode analysis.

Rather than having to switch from one application to the next for different types of analysis, the new HyperLynx tool now offers 2D/3D signal and power integrity analysis in a single application, with one GUI. Users can simulate a critical SERDES channel one minute, and then by selecting a single new menu item, switch to analysis of a large power net's decoupling.

The product now combines a super-fast geometry extraction engine and advanced materials modeling (for wideband dielectrics, copper roughness, etc.) to produce highly accurate simulations. The new HyperLynx release implements a 'decompositional' analysis flow mixing 2D and 3D solvers to reduce simulation time by orders of magnitude compared to full-wave 3D.



The 3D engine is deeply integrated, so the user never has to learn the intricacies of a full-wave-solver environment. This integration ensures that signal and power structure geometries are passed; electromagnetic (EM) ports are formed; simulations are run; and S-parameter results are incorporated into time-domain simulations – automatically.

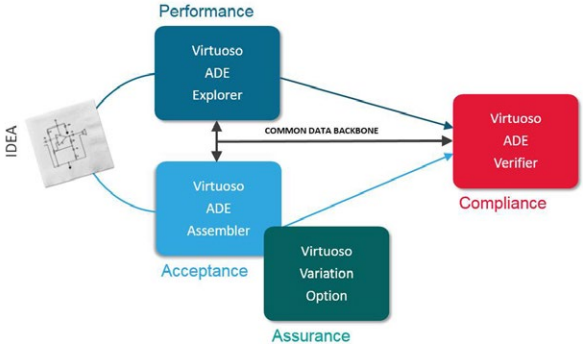
Tuning raw simulation capabilities to the specific requirements of standard interfaces and protocols (like DDRx memory and 100-Gb/s Ethernet SERDES) eases the user's burden and provides streamlined, summary pass/fail judgment on entire interfaces. The HyperLynx wizard for DDRx memory interfaces pioneered easy setup, automated whole-bus simulation, and consolidated results reporting – and is now extended to DDR4 and LPDDR4 interfaces.

In the SERDES arena, protocols that support Channel Operating Margin (COM) allow checking the quality of links based on a specific, complex set of simulation steps for a single pass/fail number per-channel. The new HyperLynx tool is believed to be the industry's first robust commercial implementation of COM for 100GbE signaling, with simulation details fully automated.

Mentor Graphics
www.mentor.com

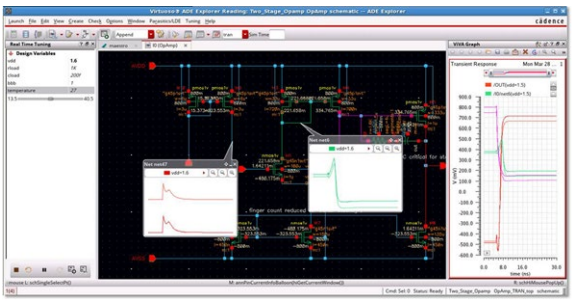
Cadence to accelerate analog verification

Cadence Design Systems has unveiled its next-generation Virtuoso platform, promising designers an average of 10X performance and capacity improvement across the platform. The updated platform includes new technologies within the Cadence Virtuoso Analog Design Environment (ADE) and enhancements to the Cadence Virtuoso Layout Suite to address requirements for automotive safety, medical device and Internet of Things (IoT) applications.



The next-generation Cadence Virtuoso ADE product suite addresses the challenges that come with the emergence of new industry standards, advanced-node designs and the requirements for system design, enabling engineers to fully explore, analyze and verify designs to ensure that design intent is maintained throughout the design cycle. Enhanced data handling provides up to 20X improvement in waveform loading and a 50X improvement in versioning and loading set-up files with databases in excess of 1GB. The suite's key technologies include:

Virtuoso ADE Explorer which allows fast and accurate real-time tuning of design specs, provides pass/fail datasheets and delivers a complete corners and Monte Carlo statistical environment for detecting and fixing variation problems



Virtuoso ADE Assembler which enables engineers to analyze their designs under various process-voltage-temperature (PVT) combinations; also offers GUI-based verification plans so designers can easily create conditional and dependent simulations

Virtuoso ADE Verifier which provides a substantial technological advancement in analog verification, offering an integrated dashboard that lets engineers easily verify that all of the blocks are contributing to the overall design specifications.

And Virtuoso Layout Suite enhancements that address the most complex layout challenges by offering accelerated performance and productivity for custom analog, digital and mixed-signal designs at the device, cell, block and chip levels. The suite's features improved graphics rendering, offering from 10X to 100X accelerated zoom, pan, drag and draw performance on large layouts. An interactive pattern manipulation flow makes real-time customization of the Module Generator very visual and simple; it now supports synchronous clones, which are layout elements with identical physical properties—like width and length of transistors—that the layout designer can layout once and reuse. The new Pin-to-trunk routing capabilities can enhance routing productivity by as much as 50 percent.

Cadence
www.cadence.com

Photonic circuit design, coming of age in a fabless ecosystem

By Iñigo Artundo

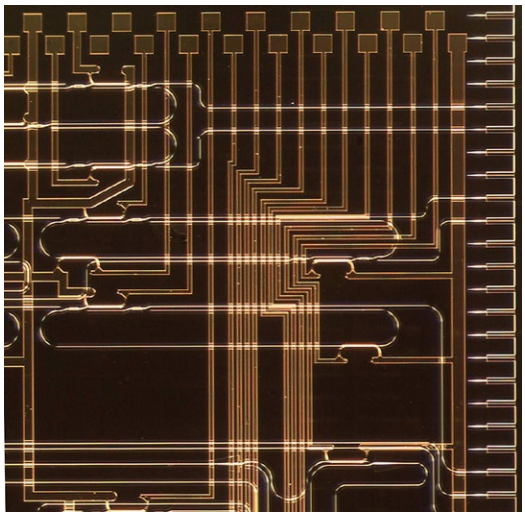
Optical integration is a technology that enables the mi-niaturization of multiple optical components like lasers, photodetectors, splitters or filters into a single photonic integrated chip. While it is still lagging about 30 years behind electronic integration in terms of maturity, it is a quickly evol-ving technology. It experienced its greatest development at the telecom bubble around 2000, where millions of passive optical components for fiber networks started to be integrated into planar lightwave circuits (PLC) made out of silica.

Nowadays, there are several mature material platforms available for fabless chip development, each of them excelling at different features: PLC because of its low loss and low cost passive circuits, silicon (Si) because of its compactness and CMOS compatibility, indium phosphide (InP) because of its capability of generating and amplifying light on a chip, and silicon nitride (Si_3N_4) because of its low loss and compactness.

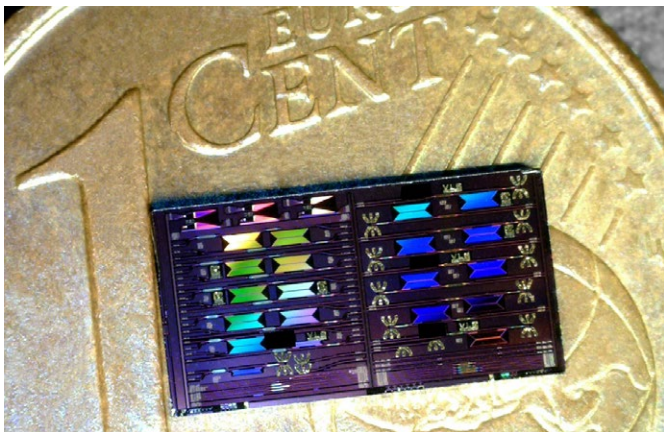
While InP and Si platforms are usually optimized to operate at the optical fiber telecommunication wavelength ranges of C-band (around 1550 nm) and O-band (around 1310 nm), PLC and Si_3N_4 can also work on the visible wavelength range, down to 400nm where many sensing and biomedical applications operate.

Once the material platform has been selected to meet the requirements of the target application, designers must select a specific foundry, or let an experienced design house like VLC Photonics assist them in choosing the most appropriate one. The design of a photonic integrated circuit starts by solving the optical modes that will be guided along the circuit depending on the waveguide geometry.

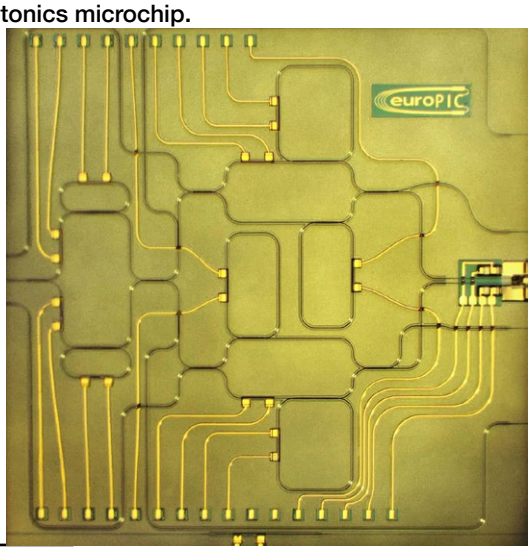
A thorough frequency domain analysis is usually performed at this stage, to calculate optical parameters like dispersion, group velocity, group index, propagation loss, effective refractive index, etc., considering certain boundary conditions (periodic, symmetric, asymmetric, metallic, etc.). Common methods for this are FD (Finite differences), FMM (Film Mode Matching), FEM (Finite Element Method), Correlation Method or Gaussian mode fiber solver, and there are several commercial software tools that implement them, like PhoeniX Software or Photon Design.



Photonic integrated circuit fabricated in Si_3N_4 for sensing applications with metallic micro-heaters.



Compact interferometers for quantum optics integrated on a silicon photonics microchip.



Complex microwave photonic integrated circuit layout in InP platform.

The next step is the propagation of these optical modes along the components that compose the circuit. While there are several methods to do this (BEP, Eigenmode expansion, transfer-matrix, split-step), the two most common ones are the Beam Propagation Method (BPM) and the Finite Differences in the Time Domain (FDTD).

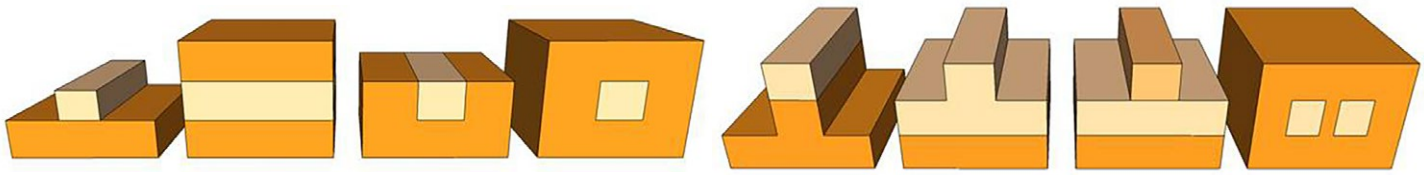
The first is used for light propagation in slowly varying non-uniform guiding structures (e.g. tapers, bends, couplers) and implements a uni- or bi-directional propagation of the total field (not mode fields), either scalar or vectorial, under a paraxial approach.

The second FDTD method is a discrete representation of time-dependent Maxwell's equations on a grid, and a wide bandwidth response can be extracted in a single simulation by Fourier transformation of the time-varying response of the system to some input. It is a truly omni-directional method, but it is very computational intensive and it usually requires heavy optimizations.

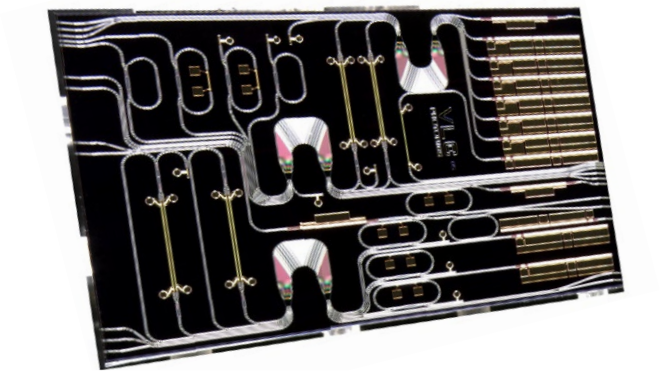
Once these two steps are done, complete circuit simulation can be done either on the time or frequency domains. This not only allows for the functional design verification of the photonic circuit, but also enables on-chip optimization of the components and their connectivity, the evaluation of tolerances and virtual experiments.

Again, there are several commercial tools that allow for this, like Filarete's ASPIC or VPIcomponentMaker, and design houses can again help with the selection of the most appropriate tools for simulating each stage, or

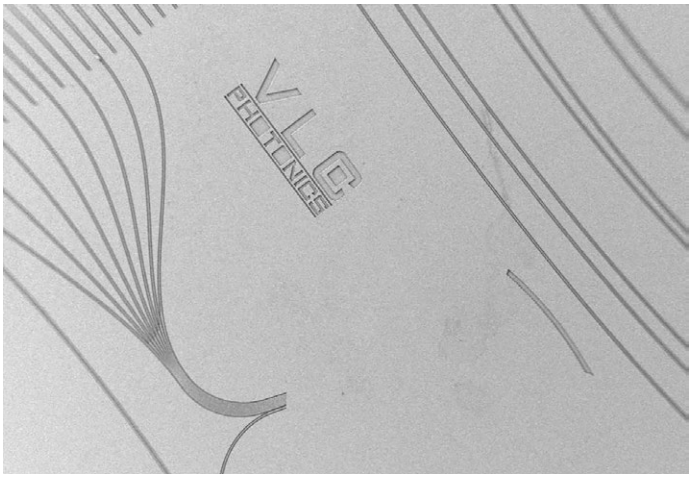
Iñigo Artundo is CEO of VLC Photonics – www.vlcphotonics.com - He can be reached at inigo.artundo@vlcphotonics.com



Different optical waveguide geometries.



Complete optical beam steering system miniaturized on a photonic InP chip.



Echelle grating WDM multiplexer for optical datacom, developed in silicon photonics.

can take care of all the required modeling and simulation works externally.

The last step consists in laying out the circuit in a photonic CAD tool that outputs a standard GDSII file with hierarchical layers. It is very important to make use of a parametric chip and mask layout, as this avoids any manual drawing or placing mistakes that affect continuity, and eases the routing work. Most photonic foundries provide a Process Design Kit (PDK) that implements the most common building blocks available on their platforms, like straight waveguides (strip and rib), bends, multimode interference couplers, grating couplers and edge couplers to interface with fiber ports, and active components like photodiodes, semiconductor optical amplifiers, modulators, heaters and DBR or DFB lasers.

Such PDKs use standard languages as well as a unified architecture through the PDAflow standard to enable interoperability among multiple EDA vendor tools, and the building blocks included in them are usually included as parameterized device layouts, also referred as pCells.

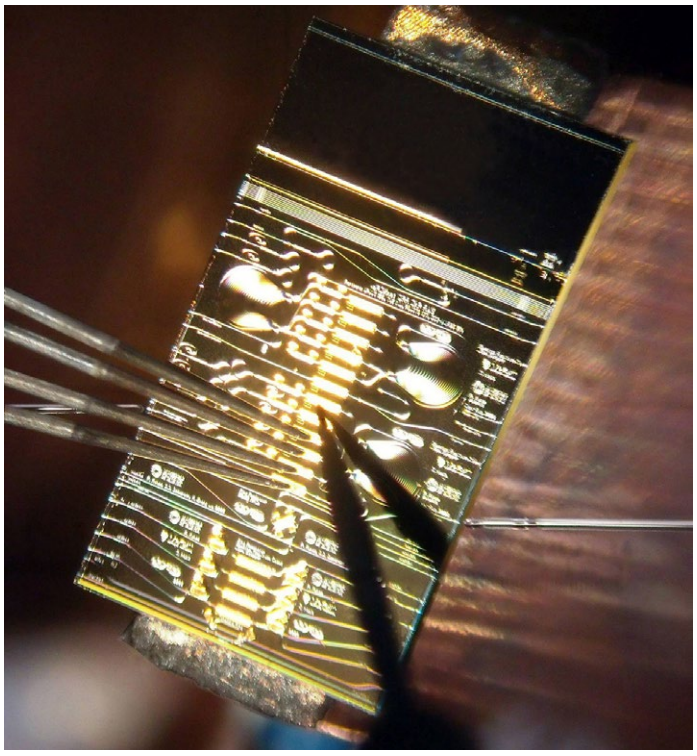
Design houses also provide their own design libraries as a complement to foundry PDKs, and can assist on design validation and rule checking, which is critical to de-risk the complete development given the large timescales and investment required in manufacturing a photonic chip.

Overall, the whole design process is finalized not only when the layout is delivered to the foundry, but when optical characterization is made on the fabricated dies afterwards, and design models are fed back into the simulations, to verify system functionality and fabrication tolerances.

This is a critical stage for iterative optimization of a photonic circuit when developing any complex system that eventually needs to go into production. When the number of fabricated dies exceeds a few units, it is recommended to rely on automated characterization setups and measurement equipment provided by test houses, so as to speed up the process and have reliable and consistent information.

Finally, there are many other considerations to be taken into account on the design of a photonic integrated circuit, like testing requirements, packaging standards or best practices, and special design requirements, shortcuts, and optimizations associated with each specific foundry.

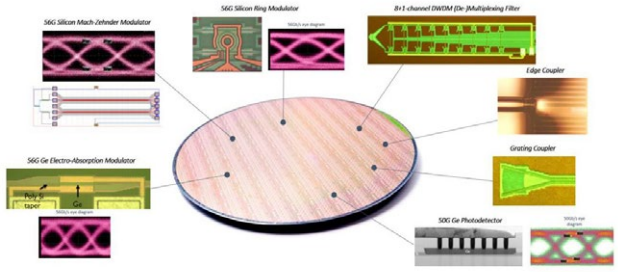
As a design house providing not only design but test services, VLC Photonics can support the development of any photonic integrated circuit in all main material platforms, given its large experience in the complete fabless ecosystem over the last decade.



Optical chip characterization is critical to validate design functionality and fabrication tolerances.

Silicon photonics platform supports 50 Gb/s NRZ optical lanes

Nanoelectronics research center imec has improved various key building blocks of its wafer-scale integrated silicon

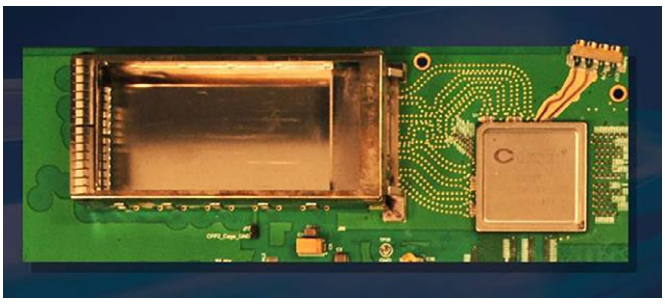


photonics platform (iSiPP), enabling the iSiPP device portfolio to support 50 Gb/s non-return-to-zero (NRZ) lane rates. This is an important milestone for the realization of high data rate silicon integrated optical interconnects targeting high density, high bandwidth, low power telecom and datacom transceivers, as well as for low cost large volume applications such as sensors or LiDAR.Through process and design optimizations, imec has improved the operating speed of the silicon based traveling-wave mach-zehnder modulators and ring modulators to reach 50 Gb/s NRZ lane rates. In addition, a C-band GeSi electro-absorption modulator was developed with electro-optical bandwidth beyond 50 GHz, enabling NRZ modulation at 56 Gb/s and beyond. All modulator types can be driven with competitive drive voltages of 2 Vpp or below, enabling compatibility with power efficient CMOS driver circuits.The responsivity of the high-speed Ge photodetectors has been improved to 1 A/W, enabling highly sensitive 50 Gb/s NRZ receivers both in the C-band and the O-band. Also, edge coupling structures were developed for broadband optical coupling to high-NA and lensed fiber with less than 3dB insertion loss in the C-band. Moreover, designers can exploit the superior patterning fidelity provided by 193-nm lithography, enabling robust active and passive waveguide devices.The 50 Gb/s components are included in imec's 200mm silicon photonics multi-project wafer (MPW) offer, and are supported by a Process Design Kit (PDK). The MPW service is available via Europractice IC service and MOSIS, a provider of low-cost prototyping and small volume production services for custom ICs. Imec's active iSiPP50G run is now open for registration (deadline June 28th 2016) with first wafers out in January 9th 2017.Imec also provides technology customization options with dedicated wafer fabrication services supported by a PDK. This service enables the use of full-size reticles, delivery of full wafers, and access to specialty modules enabling high efficiency integrated heaters, MOSCAP devices and flip-chip assembly amongst others.The PDK's have been validated with silicon data, based on a minimum of two process runs for most of the components, and describe the process and device performance statistics. They are supported in various EDA environments and include DRC, supporting first-time right designs.

imec
www.imec.be

16nm coherent optical networking platform supports 6.4 Tbps per line card

ClariPhy has announced what the company claims to be the world's first complete 16nm complete ADC and DAC platform



enabling 64QAM modulation to achieve up to 70 Tbps per fiber and more than 50% power reduction to double system capacity. The new coherent test platform establishes a critical foundation for ClariPhy's forthcoming LightSpeed-IIITM family of SoC devices that will enable 70 Tbps per fiber with more than 400G per wavelength, while driving more than 50 percent power reduction. The platform's full-speed 4-channel ADC and DAC supports variable baud rates to enable a true FlexCoherent solution programmable up to 400G per wavelength. The reference design is the result of a close collaboration between ClariPhy and leading ecosystem partners and includes components from Fujitsu Optical Components (FOC), InPhi, Macom and NeoPhotonics.

ClariPhy
www.clariphy.com

40W LED module for general lighting requires no heatsink

Slovakia's FuturoLighting has introduced an extension to the company's range of LED modules. The square DC LED module offers a ready-made solution for fixture producers and hobbyists.

The module is populated on 210x210 mm metal core PCB, assembled by 144 mid-power LEDs according to user selection. The module does not require an external heatsink because power dissipation is distributed among numerous LEDs. The module reaches more than 5000 lm. There are several possible configurations for connecting the module enabling the module to reach above 20 000 lumen in total for certain formats.

Connection of the modules to power supply is realized by poke-in terminals (respectively soldering pads, according to request). The module is suitable for applications in low bay, high bay, wall washers and plant growing. LED module is customizable where customer can select LED brand, CCT, CRI, flux bin, and drawing current as well.

FuturoLighting
www.futurolighting.eu

IC drives up to six LED strings at 93.5% efficiency

The ARC1C0608 IC is a LED driver that is so efficient that it is able to save 0.5W (in a typical 2W host platform) when deployed in backlights for tablets and other smart mobile devices, according to manufacturer Arctic Sand Technologies. Arctic Sand IC's feature TIPS (Transformative Integrated Power Solution) a patented 'staged pipeline' architecture that effectively reduces dependence on inductance, inherently lowers EMI and ripple.

The ARC1C0608 LED driver has six integrated programmable current sinks, integrates all MOSFETs, its control and driver circuitry, and features state of the art dimming options within a tiny WLCSP-35 package. The TIPS boost architecture delivers LED efficiency levels of 93.5% peak for up to six LED strings at 3.8V input voltage.The chip runs off a single cell Li-Ion battery input voltage of 2.7V - 5.5V and delivers up to 30V output for maximum flexibility in the assignment of LEDs to strings and selection of LED forward voltage. The IC includes extensive fault protection including over-current, output over-voltage and under-voltage protection, LED open and short protection (eliminating the need for an external disconnect switch). An I²C 6.0-compatible serial interface operating at up to 1MHz is included.The IC facilitates linear, PWM, or hybrid PWM dimming with either linear or logarithmic function, and phase-shifted PWM dimming can be employed among active strings to eliminate audible noise.

Arctic Sand Technologies
www.arcticsand.com

Full colour LED cluster packs 7 individually addressable dies

LED Engin has announced a 7-color, high power LED cluster, the LZ7-04MU00 emitter, aimed at stage or architectural lighting with sophisticated effects over the full colour spectrum.Its RGBW die are complemented by phosphor-converted (PC) amber, cyan and violet to provide richer, wide-ranging colour effects. PC amber delivers the same saturation as regular amber but with 5 times the flux at temperature, cyan fills the spectrum gap between blue and green, and violet enables black or crisp white lighting effects. With a 7x7mm footprint, the flat lens LZ7 emitter comprises 7 individually addressable dies assembled onto a 3.8mm light emitting surface and capped with a low profile glass lens. This ultra-thin construction means that mixing rods can be positioned as near as possible to the die to maximize coupling efficiency.LED Engin's proprietary multi-layer, multi-channel substrate boasts a thermal resistance of only 1.4°C/W and dissipates up to 20W effectively. RGBW individual dies can therefore be driven, one at a time, to a maximum current of 1.5A. Alternatively, a single amber, cyan or violet die can be driven at up to 1A. In a third operating mode, all dies can be driven simultaneously at 850mA.

LED Engin
www.LEDEngin.com

1.2MP image sensor has global shutter

1/3-inch format device delivers the functionality and robustness for automotive, barcode scanning, and virtual reality cameras. On Semiconductor (Phoenix, Arizona), has introduced the AR0135 global shutter CMOS image sensor. This 1/3-inch format, 1.2 MP imaging device has been designed to automotive imaging, barcode scanning, and virtual reality and 3D depth sensing. The global shutter allows the camera to avoid rolling shutter artifacts and aids synchronization with pulsed light sources. The AR0135 sensor has 10x lower dark current and 4x higher shutter efficiency compared with the previous generation products. On Semi did not identify the products it is comparing against.

This 1280 x 960 resolution device is capable of 54 frames per second (fps) at full resolution and 720p at 60 fps. AR0135 has dedicated flash and trigger pins used to control of LED light sources, and synchronize multiple sensors for stereo camera applications. An on-chip temperature sensor and statistics engine enhance the diagnostic and control capability of the camera system. The AR0135 also provides the flexibility of both parallel and serial (via a four lane HiSPi interface) outputs. The AR0135AT is tested and qualified to meet the AEC-Q100 Grade 2 temperature range of -40 to 105°C, while the AR0135CS supports the standard temperature range of -30 to 70°C. Both are offered in a BGA-64 package or as a bare die. Engineering samples are available now, and the devices will be in production in 3Q16.

On Semiconductor
www.onsemi.com

Winbond stacks NOR and NAND dies in 8-pin memory package

Winbond Electronics has expanded its flash product portfolio with the introduction of a family of stackable SpiFlash

memories. The SpiStack W25M Series allows the "stacking" of homogeneous or heterogeneous flash, thus achieving memories of varying densities for code and/or data storage, while providing designers with the flash solutions most appropriate for their design requirements in the well-established 8-pin package. Additionally, W25M memories feature the popular, multi-IO SpiFlash interface and command set. SpiStack homogeneous memories are achieved by stacking SpiFlash dies - for example, two 256Mb dies combining to form a single SpiFlash 512Mb NOR memory - in the industry-standard 8-pin 8x6mm WSON package. This stacked product, W25M512JV, is also available in the widely used 16-pin SOIC or 24-pad BGA packages and is sampling now. SpiStack heterogeneous memories call for the stacking of a NOR memory with a NAND die, such as a 64Mb SpiFlash NOR blended with a 1Gb Serial NAND die, which gives designers the flexibility to store code in the NOR die and data in the NAND memory. Winbond will offer multiple SpiFlash configurations, each with density ranging from 16Mb to 2Gb, to be stacked with any combination of NOR and NAND dies.

Winbond
www.winbond.com

300W PMBus compliant DC-DC converter in a 1/8th brick

The Murata Power Solutions DBE series of 300 Watt fully regulated digitally controlled DC-DC converters come packaged in

an industry standard 1/8th brick format.The footprint conforms to the Advanced Bus Converter (ABC) Digital standard as specified by the AMP Group industry collaboration. Accommodating the internationally accepted telecommunications network voltage (TNV) standard input range from 36 – 75 V_{in} and providing a PMBus compliant digital system interface, the DBE series is designed for use in distributed power and intermediate bus applications. A 32-bit ARM processor contains Murata proprietary firmware designed specifically to control and manage the converter's operation.The DBE series comprises three single output models providing the nominal output voltages of 3.3, 5 and 12 V_{out}. These highly efficient converters, typically 94.5% efficient ($12V_{out}$ model), offer basic 2250 VDC isolation as required for some PoE applications. Two or more $12V_{out}$ units can be connected in parallel to achieve load sharing for increased Pout or N+1 operation.The PMBus interface facilitates power management features that allow power system architects great flexibility to control critical operating parameters.

Murata Europe
www.murata.com

Radar development kit gets you started in remote sensing

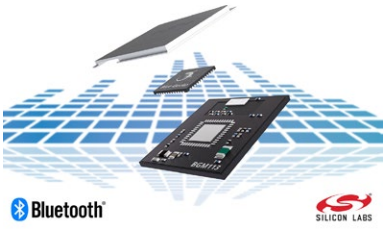
This month, Omniradar is giving away the OMDEVKIT-60A, a radar development kit worth 4000 euros, developed as an

evaluation platform for the company's RIC60A 60GHz radar chip. The chip integrates two receive antennas and one transmit antenna which allow for the simultaneous detection of position, speed and angle of arrival for multiple objects. Working in the 60GHz ISM band with a bandwidth up to 7GHz the IC offers a cost-effective solution for many consumer and industrial applications such as presence detection outdoor and indoor, gesture sensing, distance sensors, gauging, speed sensors for sports and security, or automotive radars. Based on an advanced SiGe process, the chip features an integrated oscillator, PA, LNA, IF amplifiers and AD-converters, all in a 7.0x7.0x1.2mm LGA package. The kit consists of a sensor board containing the RIC60A and an USB-interface board. Also included in the package are a USB cable and a USB stick containing sample MATLAB scripts for Doppler and FMCW radar measurements and algorithm development on a PC, a software GUI for programming the RIC60 (through SPI), code, package footprint, chip specifications and an application note.

Check the reader offer online at
www.electronics-eetimes.com

9.2x15.8x1.83mm Bluetooth module supports links up to 50m

Silicon Labs has introduced a fully integrated, pre-certified Bluetooth module, only 9.2x15.8x1.83mm in size, that delivers



up to 3 dBm of output power for applications requiring up to a 50m range.The Blue Gecko BGM113 module combines a 2.4 GHz Blue Gecko wireless SoC (2.4 GHz transceiver with a 40 MHz ARM Cortex-M4 core, 256kB flash and 32kB RAM) and a high-efficiency chip antenna into a complete, ready-to-use system. BGM113 modules are pre-loaded with Silicon Labs' Bluetooth 4.1-compliant software stack and are field-upgradable using device firmware upgrades to Bluetooth 4.2 and beyond. The BGM113 module frees developers from complex RF design or protocol decisions, allowing them to focus on the end applications.As a pre-certified solution, the module minimizes the time, effort and risk required for FCC/CE/IC certifications in North America and Europe and certifications for Japan and South Korea.The device is supported by Silicon Labs' Simplicity Studio development platform and wireless software development kit.

Silicon Labs
www.silabs.com

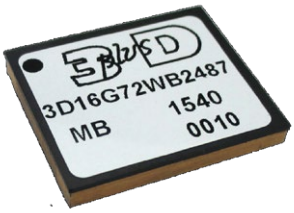
Temperature sensor ICs monitor up to four channels with ±1°C accuracy

The MCP990X family of System Management Bus (SMBus) temperature sensor ICs from Microchip can monitor up to four channels in cold, outdoor and industrial low-temperature applications ranging from freezers and refrigerators to base stations and remote radio units. With ±1°C maximum accuracy for both external and internal diode temperatures from -40°C to +65°C, the ICs include remote diode temperature measurement with resistance error correction that compensates for voltage drops from connectors and long board traces, enabling accurate readings of up to 20 inches away from the IC. Injected system noise from components such as DC-DC converters and backlight inverters is also minimised with a sample-frequency hopping filter, allowing for easier placement and routing. The combination of these features with options for dual-, triple- and quad-channel temperature monitoring provides for a wider range of measurement opportunities for an entire system with a single IC. The chips come in an 8-pin, 2x2mm WDFN package for the dual-channel version (MCP9902) and in a 10-pin, 3x3mm DFN package for the MCP9903 triple and MCP9904 quad temperature sensors.

Microchip
www.microchip.com

16Gb DDR3 memory module comes with 72-bit bus

3D PLUS has expanded its product line with the 3D3D16G-72WB2487, a 3D memory stack module with a footprint of 27.2x18mm, 57% smaller than alternative discrete solutions where components are placed next to each other.Aimed at airborne and military applications, the module provides 16Gb of DDR3 memory with a 72-bit bus, while integrating decoupling filters and termination resistors in a 223 pins BGA package. It delivers the benefits of an unbuffered SO-DIMM solution while resolving the needs for reliability and miniaturization. Like all 3D PLUS modules, the 3D3D16G72WB2487 is available in industrial (-40°C +85°C) and military temperature range (-55°C +125°C), ensuring stable operation in harsh environments. Data transfer speed is up to 1600Mb/s, with the capability to transfer 64 bits of data and 8 bits of ECC in one clock cycle.Such performance can be achieved without compromising operating conditions or power budget. The 3D3D16G72WB2487 design is based on the SO-DIMM JEDEC standard: the memories are routed with a fly-by topology to enable the higher speed of DDR3. The recommended decoupling capacitors and terminations resistors for command, control and address signal are all included; making the integration of the 3D PLUS module as easy as inserting a DIMM module in a PC.



3D PLUS
www.3d-plus.com

Real-time RF analyzers perform 20 GHz scans in less than 20 ms

The Spectran V5 real-time RF spectrum analyzers from Aaronia USA are designed to capture even the shortest of signal transmissions.With 20GHz scans or logs performed in less than 20ms (requiring option 160), the instrument is claimed to be the world´s fastest handheld RF spectrum analyzer. Available in 4 different versions in a variety of frequency ranges, the V5 comes with the RTSA PC software, supporting both powerful field analysis and benchtop laboratory work.The USB8000 series (USB “X” version) of RF spectrum analyzers feature the same specifications as the HF8000 series, but are housed in a milled aluminium case for bench or desktop use. The XFR V5 PRO is a portable, rugged unit whilst the RSA 8000 V5 comes in a standard 19 inch rack mount, covering 9 kHz to 20 GHz. The latter features remote control via USB/Ethernet and includes real-time and logging software for Mac-OS, Linux and Windows.

Aaronia USA
www.AaroniaUSA.com

1.2x1.2x0.5mm 3-axis magnetometer delivers ±1º accuracy

Delivered in a 1.2x1.2x0.5mm BGA package, MEMSIC’s MMC3630KJ series magnetometer includes an integrated monolithic 3-axis AMR sensor and a signal conditioning ASIC in one device. The MMC3630KJ is a breakthrough design in AMR technology with the ability to reach ±30G range, and more than 5x better noise level compared to other technologies, claims the manufacturer. With 600Hz magnetic sensing bandwidth, the chip is able to provide better than ±1°accuracy in eCompass applications. The design also has drastically lower system level power consumption and processing time. The series also includes a self-degaussing feature, which can eliminate the output drift due to temperature change and residual magnetic from ambient magnetic field. The series also includes an interruption feature, which can be used for motion detection and data acquisition ready notifications to lower system-level power consumption.

MEMSIC
www.memsic.com

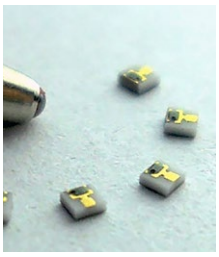
Energy-recovering modular rack-mount ATE DC load

Incorporating an inverter that returns up to 93% of power back to AC source, Intepro Systems' ELR 5000 modular, programmable DC load is housed in a 6U, 19-in. rack enclosure and can accommodate up to 10 completely self-contained, fully-programmable DC load modules with 320W nominal power, each. The modules can be used separately or in parallel, providing up to 3.2 kW. Up to 93% of the load power is returned to the source, offering energy savings in production test of DC power sources. The ELR 5000 Series offers three common regulation modes: constant voltage, constant current and constant power. Modules are offered in two input voltage/current ranges: 0-80V/0-25A and 0-200V/0-10A. Each module is equipped with touch-panel controls and a built-in sequence generator. A USB port provides flash-drive access to upload and save test sequences. An Ethernet/LAN port enables remote control of all functions via SCPI language or Modbus protocol. The company says the system provides a combination of fully-programmable, modular loads in a compact rack-mount system with the added benefit of energy recovery, a cost-effective alternative to the expensive cooling systems used by conventional air- and water-cooled loads to dissipate energy as heat.

Intepro Systems
www.inteproATE.com

DC to 60 GHz chip termination resistor targets wireless backhauls

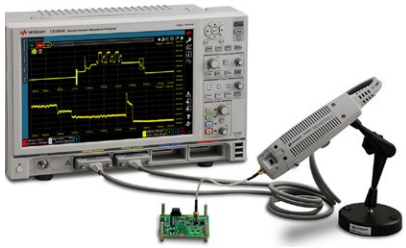
Barry Industries has introduced an ultra-broadband, DC to 60 GHz chip termination for microwave applications. The uniquely designed TV0404FA-50R0JN-91 has been third-party tested to show a typical return loss of 18.5 dB or better over a DC to 60 GHz bandwidth. The TV-0404FA-50R0JN-91 is a compact, 0404 (1.016- x 1.016-mm) size chip constructed of robust thick film on alumina with a wire-bondable input pad and epoxy or solderable ground. This 50 ohm impedance device is RoHS/REACH compliant and is rated at 250 mW on a 100°C mounting surface temperature. The TV0404FA-50R0JN-91 is available in bulk or tape and reel packaging for high-speed pick and place assembly.



Barry Industries
www.barryind.com

Analyzer visualizes previously undetectable wideband, low-level current waveforms

Keysight Technologies, Inc. has introduced what the company claims is the world's first analyzer enabling a minimum of 100-pA level dynamic current measurements with a maximum of 200 MHz bandwidth, 1 GSa/s sampling rate and 14- or 16-bit wide dynamic range.The Keysight CX3300 Series Device Current Waveform Analyzer claims to be a new category of instrument that is ideally suited for researchers struggling with high-speed transient current measurements during advanced device characterization and engineers working to reduce power/current consumption in low-power devices.Characterizing advanced devices and evaluating low-power devices are challenging tasks; ones that require engineers to measure high-speed (over 1 MHz) and low-level dynamic current (below 1 µA). However, the existing methodology for this measurement is plagued by many issues – a large noise, voltage drop, limited dynamic range, bandwidth – and as a result, low-level dynamic current often goes undetected and unmeasured. Keysight's CX3300 analyzer overcomes this limitation by enabling the simultaneous measurement of wideband and low-level current waveforms. By providing a 14-bit or 16-bit wide dynamic measurement range, a single instrument can meet a wide range of measurement requirements without using multiple instruments. A graphical user interface on a WXGA 14.1-inch multi-touch display, and advanced measurement and analysis software, make previously difficult low-level current waveform measurements and analyses dramatically efficient and easier to make.Using the CX3300 analyzer, researchers can now measure transient current even if the pulse width is very narrow (less than 100 ns). This capability is beneficial for device engineers developing semiconductor or advanced memory devices because it allows them to visualize previously unmeasurable waveforms. Current consumption waveforms can also be clearly captured at any point in time, whether the device is in its sleep/standby or active state. By being able to clearly see how a device consumes power, engineers are better able to quantitatively evaluate and reduce a device's power /current consumption.In addition to using the CX3300 analyzer to measure dynamic current, the analyzer can also be used as a debugging tool, enabling deep-dive and accurate evaluation during R&D. Doing so, drastically increases R&D efficiency and accelerates the development process by shortening turn-around-time.



Keysight Technologies, Inc.
www.keysight.com

10-Gbit LAN transformers support PoE

Würth Elektronik eiSos GmbH & Co. KG (Waldenburg, Germany) is now offering LAN transformers for speeds of up to 10 Gbit/s and supporting Power over Ethernet (PoE) up to 100W and currents up to 1A per channel. These transformers have an extended temperature range (-40 to +85 °C). Typical applications include the quasi real-time transmission of high-definition video data in the home entertainment sector or for video displays in the public space. The extended temperature range means the modules are also suited for industrial applications. Free-of-charge samples are available on request; all products are directly available from stock.

Würth Elektronik eiSos GmbH & Co. KG
www.we-online.com

Fear not the cobot

By Jonathan Wilkins

Discussing the newest and perhaps most exciting realm of industrial robotics: collaborative robots.

The world's first industrial robot was an idea conceived after a conversation about science fiction novels between inventors George Devol and Joseph Eagleburger in 1954. Six years later, Unimate had secured its place in the robotic hall of fame as the world's first industrial robot.

It was then put to work on the General Motors assembly line in 1961. Inevitably, the public were sceptical of the safety issues surrounding Unimate. And with only Gort, the laser-firing robot from the 1950's thriller "The Day the Earth Stood Still" for reference, who can blame them?

But after 50 years of practice, today's industrial robots are a much less scary affair.

The term 'collaborative' simply describes robots that can operate safely alongside their human counterparts on the factory floor. Traditionally, robotic machinery was constricted to work inside robotic work cells with physical barriers to protect human workers. Today, the new generation of robots is completely cage free. But that doesn't mean these robots are totally devoid of health and safety features.

Unlike industrial robots of the past, collaborative robots are specifically designed to work safely around people. In fact, since ABB Robotics introduced YuMi, it's two-armed collaborative robot, earlier this year, it has been independently certified as safe to work hand-in-hand with humans on the same assembly tasks.

To prevent accidents with human workers, sensors are installed on the robot that react to human contact and monitor the location of humans on the factory floor. This way, if anybody does get too close the machinery, it automatically shuts down. What's more, the strength, speed and force of this collaborative machinery is limited to avoid causing serious injury if contact does occur.

In addition to this, many collaborative robots require little to no skill to program. Most are so simple that anybody who can use a smartphone or tablet has the ability to program them, a world away from the complex robots of just a decade ago, which required highly skilled technicians to program and watch over them while they operated.

One industry that is being transformed by collaborative machinery is automotive manufacturing.

It's no secret that the sector has always been at the forefront of industrial robotics. Since the early 1960s automotive manufacturers have been using robotic equipment but since then, a lot has changed. To keep up with the competitive nature of the industry, manufacturing lines need to be more efficient, flexible and productive than ever before.

Inevitably, many will see this advancement in robotics as a further threat to human jobs on the production line, but that's simply not true. Just as a concrete mixer is designed to help, not replace, the bricklayer, collaborative robotics are simply intended to assist the workers on the assembly line.

In fact, some experts predict that just as an engineer uses a computer to make their job easier, production line workers will use a collaborative robot to assist them with theirs.

One of the reasons BMW recently introduced collaborative robots to its assembly lines was due to the drop in motivation it saw in its human workers when they were forced to perform menial tasks all day.

With collaborative robots on hand, it freed human employees to focus on jobs that required intellect, judgment and creativity, leaving the robots to pick up the tasks that no one wanted to do.

In the past decade, robots have come a long way. From scary, somewhat threatening machines held behind intimidating safety barriers to the slick robotic technology we see today, capable of working hand-in-hand with humans.

Of the many innovative applications used in today's automotive industry, collaborative robotics is certainly one of the most exciting.

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Distributor Acal BFi has signed a new pan-European distribution agreement with MEMS sensors manufacturer Tronics to distribute Tronics' Gypro MEMS inertial sensors to the European markets. The Gypro series offers best-in-class bias stabi-lity (Allan variance) of 0.8°/h and the lowest angular random walk of any comparable gyro. Designed specifically to meet the most demanding requirements of navigation and stabilization applications, Tronics GYPRO2300 and GYPRO3300 products boast miniature size, light weight and low power consumption (25mA).

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Sensirion signs worldwide distribution with Digi-Key

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Farnell element14 is stocking Texas Instruments' MSP CapTIvate microcontroller development kit, a comprehensive, easy-to-use platform providing real-time sensor tuning, all without writing a single line of code. The kit contains a Captivate-FR2633 target MCU module, Captivate-PGMR eZ-FET with EnergyTrace technology and HID communication bridge, Captivate-ISO UART, I2C, and SBW isolation board, Captivate-BSWP self-capacitance demo (Out-of-Box Experience), Captivate-Phone mutual capacitance demo with haptics and guard channel and Captivate-Proximity proximity detection and gesturing demo.

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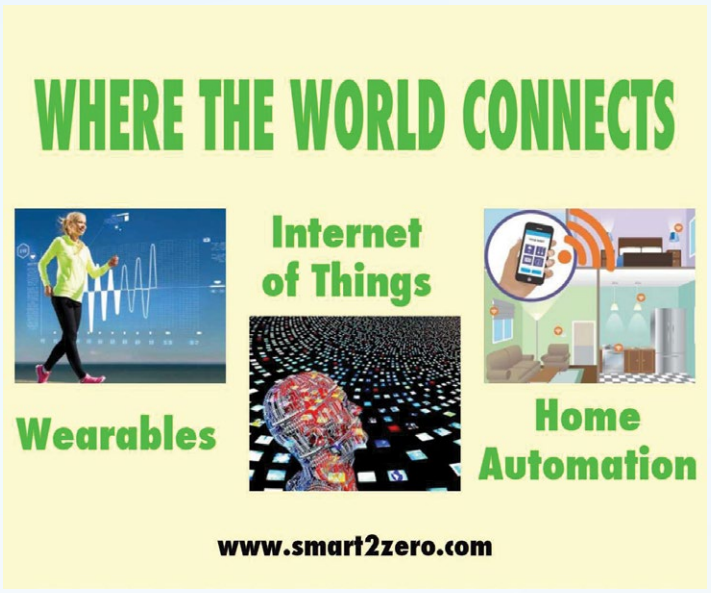

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